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This report covers the first twenty-one months of the AOSP GaAs Memory Program. The objective of this program is to utilize the performance advantages offered by GaAs integrated circuits in the areas of radiation hardness, low power dissipation and high speed for the development of a 4K bit RAM. The DARPA process development program has complemented and provided a sound basis for the initial progress made in this RAM program. Using the existing GaAs technology as a base, we have initially focused

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our efforts on process areas unique to RAMS, on evaluation of the power concentration RAM cell and on the design and fabrication of a 256 bit static memory chip.

The development of operational 256 bit memory arrays has been used on three mask sets; namely AP1, RM2 and RM3. Mask set AP1 contained preliminary RAM cell designs for verification of design concepts and layout rules while RM2, using data obtained from AP1, focused on the design, fabrication and evaluation of 256 bit RAMs. The RM3 mask set was used to initiate the processing of 3 in. GaAs wafers, and at the same time to fabricate a fully functional 256 bit static RAM.

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TECHNICAL SUMMARY

This report covers the first twenty-one months of the AOSP (Advanced On-Board Signal Processor) GaAs (gallium arsenide) Memory Program. The objective of this program is to utilize the performance advantages offered by GaAs integrated circuits in the areas of radiation hardness, low power dissipation and high speed for the development of a 4K bit RAM. The DARPA process development program has complemented and provided a sound basis for the initial progress made in this RAM program. Using the existing GaAs technology as a base, ~~we~~ the authors have initially focused ~~our~~ their efforts on process areas unique to RAMS, on evaluation of the power concentration RAM (random access memory) cell and on the design and fabrication of a 256 bit static memory chip.

The development of operational 256 bit memory arrays has been used on three mask sets; namely AP1, RM2 and RM3. Mask set AP1 contained preliminary RAM cell designs for verification of design concepts and layout rules while RM2, using data obtained from AP1, focused on the design, fabrication and evaluation of 256 bit RAMs. The RM3 mask set was used to initiate the processing of 3 in. GaAs wafers, and at the same time to fabricate a fully functional 256 bit static RAM.

Preliminary Mask Set AP1

The first mask set, AP1, was used as a test vehicle for the evaluation of design rules, measurement of device and substrate characteristics, development of megohm resistors, and performance mapping of individual RAM cells and simple arrays. The device test results obtained from this mask set revealed a number of parameters directly applicable to the design and operation of 256 bit arrays. In addition, a fabrication technique for cermet ($Cr:SiO_x$) megohm resistors was developed and incorporated into several of the AP1 wafers. In this way, cell operation using both on-chip cermet resistors, as well as external resistors, could be evaluat d and compared. The bistable operation range for the individual R. .lls as determined as a function of power supply voltage, and effects of resistor nonuniformity were measured.

Analysis of megohm cermet transistor test results indicated that this approach is a viable technology for the 4K RAM. Finally, preliminary yield data from this mask set indicated that tightened design rules with 2 and 4 μm FETs was a viable option (from a processing standpoint) for future RAM cell designs.

RAM (256 bit) Array Design (RM2 Mask Set)

Using the AP1 test results as a guide, the second mask set, RM2, was designed. In addition to the cell arrays, a preliminary design was also made for the decoder circuits. Three 256 bit arrays (with decoders) were included. These were: 1) the baseline low power cells, 2) a high power version with four times the current level, and 3) a low current version with three diodes instead of two. Another array with 224 baseline cells without decoders was also included for direct probing.

RAM Process Development

Processing of the RM2 (256 bit RAM) wafers proceeded using normal planar GaAs fabrication methods, except for two process areas which are characteristic of the low power requirements of RAM arrays; namely, control of a lower threshold voltage (0.5 V) FETs and incorporation of an additional mask level for the megohm cermet resistors. These two exceptions to the standard IC process presented minimal problems for wafer fabrication. Measurements of threshold voltages showed a standard deviation over the 1 inch wafers of less than 100 mV (with typical values in the 60 mV range), while resistor values showed a uniformity of better than ± 10%. In addition, the process monitor values such as diode series resistance and ohmic contact resistance were all within normal bounds for the wafers tested.

RM2 Performance Results and Yield

Testing of the undecoded arrays on RM2 was done using an automated probe station and a microcomputer test system. Each cell in the array was tested, and a map of the array was produced showing the locating and type of

failure encountred, e.g., failure to write "1" or "0". These failure maps were used as an aid, first in the visual inspection of failed cells to determine obvious failure causes, and then for subsequent, more thorough electrical testing.

The measurements made on undecoded 224 bit arrays provided preliminary statistics in the yield of the RM2 low power cell design. Analysis of several wafer lots showed that substrate isolation was not sufficient to provide a fully functional array. Measurements on individual FETs within a RAM cell revealed a variation in gate voltage with drain current. The results suggested a leakage path from gate to drain and thus failure of the cell. As a result, proton bombardment was used to improve the isolation characteristics of the substrate. Testing of arrays after proton isolation was employed revealed a significant decrease in the failure rate, and thus became a standard process technique for RAM arrays.

Mask Set RM3 Design and Layout

The main objective for designing mask set RM3 was to launch the processing of 3 inch diameter GaAs wafers. The 256 bit RAMs on mask set RM3 were very similar to those on mask set RM2 except for relatively small corrections and design improvements. The main changes from mask set RM2 to mask set RM3 were related to die organization and alignment marks for processing with a 10X wafer stepper on 3 inch wafers. Mask set RM2 contained a number of different versions of the 256 bit RAM, some with and some without peripheral circuits. Several versions were also included on RM3, but the number of different options was smaller. RM3 provided an opportunity to add a number of test structures consisting of portions of the peripheral circuits and single cells which were extracted from the full RAM circuits. This addition was very important because mask set RM2 lacked these diagnostic elements.

Three-Inch Wafer Processing

Prior to the fabrication of the first RM3 wafers, the entire process line was changed from a 1 inch square wafer format to 3 inch round wafers. During this time, every piece of processing equipment was either modified to accommodate the larger substrate size or replaced by new equipment. The parametric test results from the initial wafers processed on the new line showed reasonable uniformity and pinchoff control. In addition, the two extra processing steps required for RAM arrays, namely, proton bombardment and cermet resistor fabrication, were finalized during this time.

Test Results from Mask Set RM3

The results from testing wafers fabricated with mask set RM3 were important in two ways. First, the successful fabication of 3 inch GaAs wafers was demonstrated, and second, the first fully functional 256 bit RAM was fabricated. The resulting yield, however, was very low, and residual substrate leakage, resistor unbalance, speed-up capacitor unbalance, and FET threshold voltage uniformity were all investigated as possible failure mechanisms. Threshold voltage uniformity appeared to be the most sensitive parameter which may control the yield of RAM cells. The testing of the peripheral circuits showed a high degree of sensitivity to backgating, presumably due to the low threshold voltages where were used. The reduction of backgating through the use of proton bombardment allowed the complete RA to the fabrication of the first RM3 wafers, the entire process line was changed from a 1 in. square wafer format to 3 in. round wafers. During this time, every piece of processing equipment was either modified to accommodate the larger substrate size or replaced by new equipment. The parametric test results from the initial wafers processed on the new line showed reasonable uniformity and pinchoff control. In addition, the two extra processing steps required for RAM arrays, namely, proton bombardment and cermet resistor fabrication, were finalized during this time.

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Testing of Fully Decoded 256 Bit RAMs

The functionality of 256 bit static RAMs was tested using a laboratory microcomputer equipped with analog and digital outputs and inputs. The power consumption of this static RAM was typically between 200 and 250 mW. All this power consumption takes place in the peripheral circuits which were not designed for low power dissipation. The access time of individual RAM cells was also measured and found to be generally less than 10 ns with 8 ns as a typical value. The cell was also able to store a "1" or "0" with a very short (2 ns) "write" pulse, thus leaving 8 ns to the peripheral circuit for all the "write" operation.

1.0 INTRODUCTION

The objective of this program is to utilize the performance advantages offered by GaAs integrated circuits in the areas of radiation hardness, low power dissipation and high speed for the development of a 4K bit RAM. The specific motivation for the development of a low power radiation hard memory chip is provided by the increasingly difficult circuit requirements of sophisticated military electronic systems. These system requirements translate into integrated circuit device specifications never before achieved, paving new roads in the areas of device speed, device power dissipation, device complexity and density, device reliability and survivability to severe radiation environments.

Of the various device types required in defense systems, memory is the most widely utilized, and its performance often dictates the performance limitations of the entire system. The need for a fast, ultra-low power, radiation hard memory has been firmly established by all of the defense services. In particular, development of a radiation hard memory has been identified as a key device technology for the proposed Advanced Onboard Signal Processor (AOSP) Program.

The goal of the AOSP technology program is to develop a flexible, multi-mission signal processor to fulfill the processing requirements of space-based missions through the 1990's. Applications anticipated in this time frame include various space-based radars, communication systems, and electro-optical systems in support of numerous defense, surveillance and intelligence missions. The baseline design selected by Raytheon, AOSP's system contractor, is essentially a matrix of nodes referred to as Array Computing Elements (ACE) interconnected through a multiple bus network and controlled through a two level distributed software operating system. Each array computing element consists of a signal processor providing the computational capabilities and a data processor providing interaction and control functions. Different AOSP missions may require from 20 to 60 ACE units, each

with > 2 megabytes of memory resulting in a total memory capacity of 10^7-10^8 bits with power budgets less than 100 W. The AOSP system specification translates into memory device specifications in the following manner. Long mission lifetimes (> 5 years) and space-based environmental conditions require a radiation hardened device technology capable of surviving total doses in excess of 10^6 rads. Power dissipations of 0.5-1 μW/bit are required, assuming memory power allocations of from 40-70% of the total 100 W power budget. For surveillance missions, extremely large memory requirements, along with size and weight restrictions, dictate the need for very large scale integration (VLSI) in order to minimize the memory chip count. The proposed 4K memory design goals are summarized in Table 1-1.

Table 1-1
AOSP GaAs Memory Phase I Design Goals

Memory Type	Fully Decoded Random Access
Power Dissipation (Array)	< 1 μwatt/bit
Speed	τ_{acess} < 10 ns
Radiation Hardness	> 10^6 rads total dose
Storage Capacity	> 4096 bits/chip

To realize these memory requirements with a reasonable number of chips (~ 500 as an upper limit), at least 4K bit RAM chips will be required and 16K bit chips would be preferred. Silicon bulk CMOS chips could meet these complexities and power requirements (0.05 μW/bit), but the access times are not nearly fast enough to meet the desired ~ 40 ns cycle times of the AOSP processor. CMOS/SOS RAM chips, unfortunately, suffer from an increase in the sapphire substrate interface leakage currents resulting in unacceptably high static power dissipation, even when exposed to modest doses (<< 10^6 rads) of ionizing radiation. MSI and LSI circuits of Rockwell's ion implanted planar

GaAs IC technology have been shown to survive total dose irradiation of 5×10^7 rads, far in excess of the AOSP requirements. In addition to radiation hardness and low power, GaAs RAMs also offer access times of < 10 ns. While speed, power and radiation hardness would be key technological problems in the Si RAM development for AOSP, in GaAs the key issue would be complexity, i.e., achieving the capability for fabricating 4K/16K bit RAMs with workable yields in a relatively short time frame.

The program reported herein is an excellent start toward the establishment of a 4K/16K RAM technology. This initial RAM development effort has demonstrated a fully functional 256 bit RAM with access times of less than 10 ns. Three-inch GaAs wafer processing was also developed during this time, and has since become the standard for all GaAs digital integrated circuit fabrication.

The organization of this report follows a design, fabrication and test sequence for each of three mask sets. Section 3.0 describes the first mask set, AP1, which was used to design and test basic cell operation. Additionally, the new processing techniques which were required for RAM cells were also developed. Using the results of the AP1, a second mask set RM2, was implemented. This mask set contained 256 bit decoded RAM arrays and 224 bit undecoded arrays. The results from RM2 are discussed in Section 4.0. The final mask set used during this reporting period was designated RM3. It was with this mask set that the 3 in. processing line was initiated, and the first fully functional 256 bit arrays demonstrated. These results are detailed in Section 4.0.

2.0 RAM DESIGN CRITERIA AND PROCESSING TECHNIQUES

The following section describes the basic design concepts and processing techniques which were adopted early in the program in order to set a baseline for RAM fabrication. The power concentration approach was a key factor in designing for very low power, while layout design rules set the basis for cell size, and hence, bit density. As initially conceived, the wafer fabrication for both 1 inch and 3 inch wafers would follow standard Rockwell processing techniques, with the only exception being the addition of a high value resistor process.

2.1 Design Concepts

The requirements for memory size and power dissipation are extremely demanding for the AOSP processor array computing elements (ACE). Approximately 2 M bits of bulk storage is needed for each of about 20 ACE nodes, and a 100 W power budget goal has been assigned for the complete AOSP. Allowing for 40% of the power budget in memory, the static power dissipation per bit is only 1 μW. Because relatively few of the 10^4 memory chips (10-100) are actually addressed in a 15 ns system clock cycle, the standby static power dissipation of the memory chip is of far greater significance in reducing total system power than is the chip dynamic power dissipation. Thus, the emphasis in selecting a device and circuit approach for the RAM cell must minimize the static power without undue regard for reducing logic swing (ΔV_0) to reduce the dynamic switching energy ($P_D \tau_d$). This static power requirement can best be provided by the depletion-mode MESFET approach.

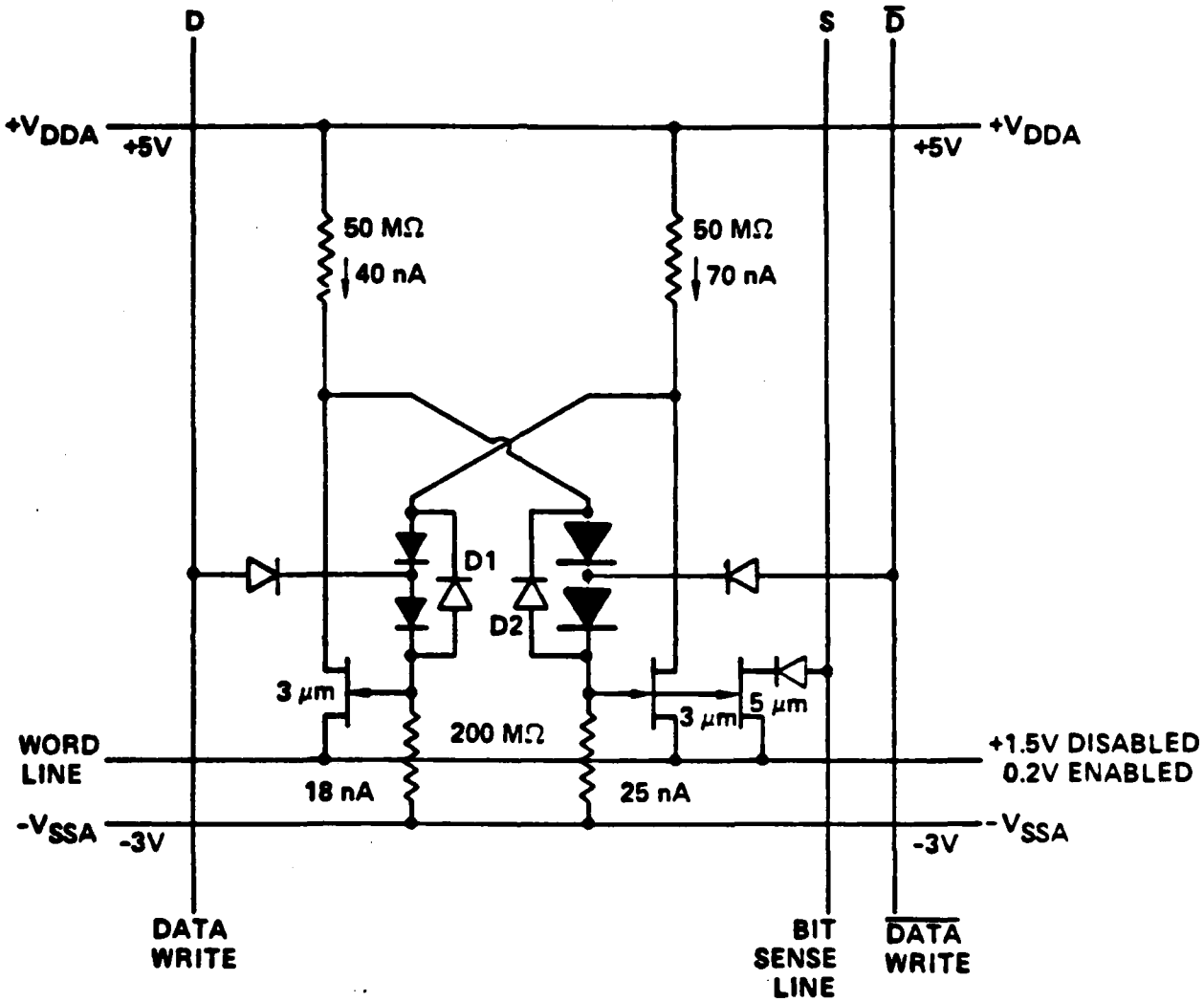
In addition, with a system clock cycle of ~ 10 ns, a relatively high speed circuit design is required while maintaining the low static power. While CMOS would be the natural choice here, MOS silicon approaches are undesirable for this application due to the limited total dose hardness of MOS. Since an equivalent complementary logic technology is not available for GaAs, an approach using only n-channel GaAs MESFETs is required. With this

approach, extremely low standby currents and modest, but considerable, access speeds must be achieved. These requirements, which seem in conflict with one another, are effectively resolved by the power concentration approach described in the following section.

2.1.1 Power Concentration RAM Cell

The key design problem for very low power, moderate access time, 4K GaAs static RAM is not so much the attainment of the $T_{acc} \sim 10$ ns speed, but obtaining the high speed operation while simultaneously holding the power levels low. Consider, for example, a 4096 cell memory array, arranged 64 x 64. The total bit sense line capacitance on one of these 64 cell columns will be of the order of 425 fF (influding overcrossings, line stray capacitance and assuming ~ 2 fF diode capacitance at each cell). For a maximum discharge or charge time of ~ 3 ns, the memory cell would be required to sink a curent of 100 μA to achieve a 0.75 V discharge of the sense line capacitance. Clearly, if all 4096 cells operated at 100 μA quiescent current levels, at V_{DD} = 3 V, the static power dissipation would be unacceptably high. Therefore, it becomes mandatory to realize sufficiently fast access time without increasing chip power dissipation.

The solution to achieving adequate readout speeds from the RAM cells without increasing their static power dissipation levels is illustrated in the cell schematic shown in Fig. 2.1-1. The idea is to concentrate power only on the bit cell being accessed, and only while that cell is being read so that the cell, at that moment, has sufficient power available to charge the bit line. This is achieved by making the RAM cell itself capable of operating at much higher current levels in readout than its static operating current levels, and then using the column address demultiplexer to make available relatively high (~ 100 μA) current levels to the cell during bit readout in that column. In the cell example of Fig. 2.1-1, the bit sense line (S), instead of being connected directly to the latch (3 μm FETs with 50MΩ pull-up resistors), is connected through a diode to the drain of a larger (W = 5 μm)



POWER/BIT = (+5)(110 nA) + (-3)(-43 nA) = 676 nanowatts/bit
MEMORY ARRAY STATIC POWER = 4096 x 676 x 10^{-9} = 2.76 mW/4K CHIP

Fig. 2.1-1 Circuit diagram for the 1 μW RAM cell. Currents shown are for a stored "zero" (left FET "off"), word line deselected (+ 1.5 V).

FET, the source and gate of which are in parallel with the 3 μm FET on one side of the latch. This 5 μm FET will be "on" only when a "zero" is stored in the latch. Ordinarily, however, this FET draws no current, since either the column is not being accessed (so that no current is supplied to the sense line, S, by the column demultiplexer), or if the column is being accessed, but not this particular row, a + 1.5 V word line voltage at the source of deselected rows will prevent the diode between the drain of the 5 μm FET and the sense line from conducting. However, if both the column and row are selected, then the word line voltage at the source of this 5 μm output FET will drop to ~ 0.5 V, and the voltage on this bit sense line will be determined by whether or not this particular 5 μm output FET is "on" or "off". The bit sense voltage will be approximately 1 V if the "zero" is stored in the latch and greater than + 2 V is a "1" is stored. The current available from a W = 5 μm, V_p = -0.7 V output FET at V_{gs} = + 0.5 V would be I_{ds} ≈ 0.4 mA, capable of achieving a voltage slew rate on a C_L = 425 fF load of dV/dt = 10^9 V/s, or requiring 600 ps to discharge the bit line by 0.6 V. This should be more than adequate for a 10 ns access time RAM.

Operation of this D-MESFET memory cell at this power level requires that the FET subthreshold currents be of the order of 10 nA. This appears reasonable as long as the logic saving is sufficient to get the gate voltage ~ 0.4 V below the "nominal" square low threshold voltage (V_p). The large logic savings available in this D-MESFET approach make that possible.

2.1.2 RAM Cell Circuit Concept Study

The first design consideration for the RAM cell, which is basically a latch circuit, is the basic size of the FETs to be used. Large FET widths (≈ 5 μm) have the advantage of being reasonably simple to fabricate with high parametric uniformity. They have the disadvantage of larger cell size and, if the total current in the latch is being established by the requirement for less than 1 μW cell, very low I_{ds}/I_{dss} ratios. Smaller FETs (down to 1 μm gate width) result in decreased cell size and operate at a more favorable cur-

rent density. However, their narrow widths (down to 1 μm) approach the feature size limitations of state-of-the-art processing, which may result in unacceptable yield and large parameter variations from device to device. The operating characteristics of the FETs and the diodes are not well-known at the low current levels involved, particularly in a densely packed chip where substrate leakage may be of significance. Therefore, both operating characteristics and device yield need to be determined experimentally for a variety of device sizes.

The second design consideration, the layout design rules, have an even greater effect on cell size, and hence bit density, than FET size. These rules are directly derived from the processing steps, and are directly tied to the resolution and layer to layer registration of the photolithographic sequence involved in fabricating the circuits. In this program, it is intended to use the tightest rules that do not degrade yield unacceptably. Yield vs design rule sizes will be determined experientally. This determination will involve the pattern to be used in the circuit (i.e., the circuit layout itself) rather than a standardized pattern, so that any proximity or shape dependent effects are automatically taken into account.

Another effect becomes important for closely spaced devices: interdevice leakage currents. These currents are generally not of concern for ordinary logic circuits operating at moderate power levels (0.2-2.0 mW/gate), but increase in importance when interdevice spacing decreases and extremely low operating currents are used. In the proposed RAM cell, the leakage currents may be greater than FET "off" currents and could even become comparable to FET "on" currents at very high circuit densities. Evaluation of these leakage currents are crucial to a well-designed low power RAM.

2.2 Processing Techniques for Low Power RAM Arrays

The realization of high speed, low power GaAs 4K bit RAM chips requires a fabrication technology capable of high process yields. The current Rockwell technology has proven to be capable of LSI complexity, and thus pro-

vides a strong basis for RAM development. As initially conceived, the RAM process would deviate only slightly from baseline processing, and as such, would not result in any major deviation from accepted processing techniques. The only area which required extensive process development was in the area of fabricating high value (megohm) load resistors. This development centered more on producing thin cermet films of the proper resistivity rather than in the actual fabriation of the on-wafer resistors themselves, since the resistor process was essentially an additional second level metal process. Details of the resistor development process are described in the sections relating to the various mask sets.

The Rockwell GaAs processing techniques have been discussed in detail elsewhere,[1] and have reached a point where 3 in. wafer processing is now standard. The following section provides a brief review of the basic process steps for RAM wafer fabrication (both 1 in. and 3 in. wafers), and is described in order of the normal process sequence, as outlined in Fig. 2.2-1., steps 1 through 11.

Localized Implantations (Steps 1-3)

The first implantation step, labeled n^-, utilizes a shallow Se implant for optimizing the FET channel regions. The second implant, called n^+, used Si in order to obtain a deeper profile suitable for the Schottky barrier switching diodes. Both implantations were used for the level shifting diode and ohmic contact regions.

Encapsulation and Anneal (Steps 4 and 5)

After completion of the implantation and mask registration steps, the photoresist mask was removed using a combination of wet chemical and dry etching techniques. The total dielectric thickness was then increased with the addition of SiO_2 over the Si_3N_4 already present in the GaAs surface.

The wafers were subsequently annealed at 850°C for 20 min in order to remove the ion implantation damage.

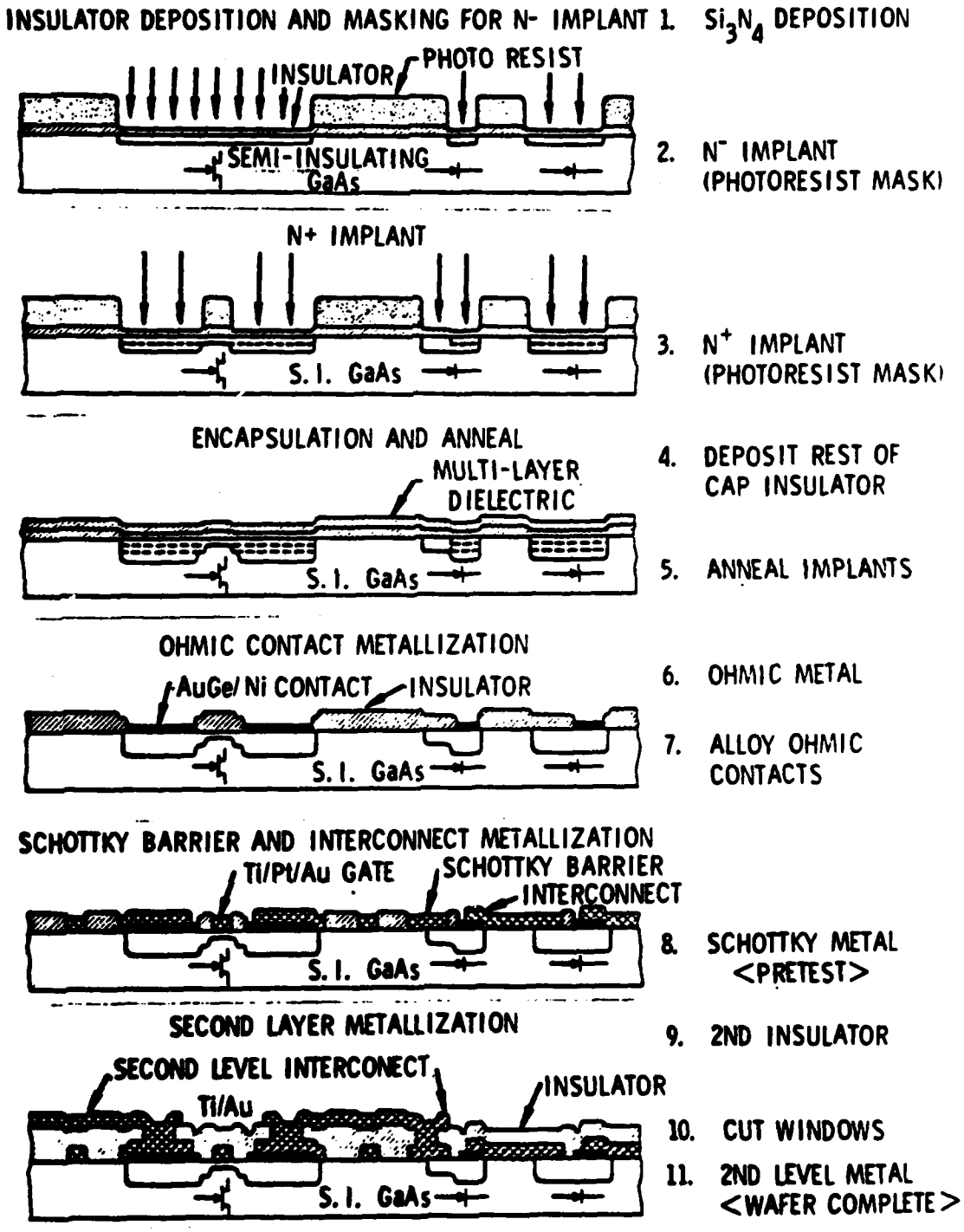


Fig. 2.2-1 Planar GaAs IC fabrication steps.

Circuit Lithography (Steps 6-8)

At this point in the process, the entire surface of the GaAs slice is still covered with a dielectric layer. The subsequent ohmic contact layer and the Schottky metalization layers, which also serves as first layer interconnect, were deposited within windows in this dielectric (as shown in Fig. 2.2-1, Steps 6-8). The ohmic contacts for the FETs, active loads and Schottky diodes used an AuGe-Pt metalization system. The circuits were fabricated by defining the desired patterns in photoresist and plasma etching the underlying Si_3N_4/SiO_2 dielectric to the GaAs surface. The desired metal layer was then evaporated and the circuits defined by photoresist lift-off.

After defining the ohmic contacts, a 1 to 2 min, 450°C thermal cycle was applied in order to alloy the AuGe ohmic metal to the GaAs surface.

Multilayer Interconnects (Steps 9-11)

The wafers were then covered with a Si_3N_4 layer in order to isolate the first-level metal interconnects from the second-level interconnects yet to be fabricated. Electrical connections from the second to the first-level interconnects were provided by via windows through the dielectric. These via windows were defined by reactive ion etching. The underlying gold-based first-level interconnect serves as an automatic etch stop for this process. The Au-based second-level interconnect was defined with an ion milling method.

3.0 AP1 MASK SET

The purpose of the first mask set, AP1, was to permit the first-cut issues of RAM devices and processing techniques to be resolved well enough so that a reasonable cell design could be made for a 256 bit array. To the maximum extent possible, this mask set was to include structures to answer or verify all anticipated parameter questions that would effect the final design of the RAM cell. The following sections will discuss the mask set layout and device considerations, the processing refinements which were needed for the development of high value resistors, and the test results which evaluated cell performance. The culmination of these efforts then led to a better understanding of low power RAM performance the subsequent design of 256 bit arrays.

3.1 Device and Layout Considerations

The conservative layout design rules that have been established for the general Rockwell GaAs IC process are not necessarily consistent with all types of circuits. These design rules have been followed to the letter in MSI/LSI circuits in which internal (gate circuit) yield is critical to achieving test parts. However, these design rules may be altered with judicious care for the sake of increased speed and/or density. For the proposed 4K RAM, the cell size should be kept to an absolute minimum, both to minimize power (by keeping line capacitances low, in part) and to keep the overall chip dimensions (with their attendant adverse affect on chip yield) as small as possible. The specific design rule limitations must be determined experimentally. A practical balance between performance and yield must be achieved through careful analysis of experimental device and circuit results. These considerations were addressed in the design of the AP1 mask set.

The two most critical device characteristics for this cell design are the FET operating characteristics below threshold (subthreshold region) and the forward voltage drop of diodes carrying very low currents. To achieve the ~ 1 μW power level in a cell, operating currents must be in the tens of nano-

amperes range, requiring verification that subthreshold currents and/or leakage currents are below this level. The voltage drop of a diode depends on current density, which can be kept high for a given current by making the diodes smaller; however, practical photolithography limits the diode to 1 μm x 1 μm. Even at this size, the operating current density is 4 orders of magnitude less than the operating current density in diodes contained in more conventional SDFL circuits. Verification that leakage currents are not of the same order of magnitude as the anticipated low operating current densities was needed.

In addition to active device characteristics, an evaluation of megohm resistors was needed in order to complete the final cell design. Since the resistor processing was an untried technology at the beginning of the program, several test structures were needed to resistor performance. During this time, the cermet film processing technique was the primary contender, although various other approaches were still being considered.

The variables in the RAM cell design are the FET size, the cermet resistor sheet resistivity and the design rule spacing. Table 3.1-1 lists the cell design variations available on mask AP1. A range of FET sizes were included in order to determine whether a lower limit will be reached where fringe effects (rather than uniform current flow) will dominate the FET behavior. With this design, processing uniformity of the various size FETs could also be determined. High sheet resistivity (20 MΩ/□), small cermet resistors were also included in the cell matrix, as well as a more readily achievable larger (5 MΩ/□) resistors. Different resistor layouts were made to achieve the design resistor value with either sheet resistivity or varying the resistor length (indicated by short or long in Table 3.1-1). Cells were also included with connections for external resistors.

Table 3.1-1

Design Variations of the RAM Cell

Cell	Device Sizes (μm)	Design Rules N = Normal T = Tightened	Resistors Int = Internal Ext = External	
1	1, 2	N	Int,short	
2			Int, long	
3	1, 2	N	Ext	
4	2, 4	N	Int, short	Included in RAM array A
5			Int, long	
6	2, 4	N	Ext	
7	2, 4	T	Int, short	
8			Int, long	
9	3, 6	N	Ext	
10	3, 6	N	Int, short	
11			Int, long	
12	3, 6	T	Int, short	Included in RAM array B
13			Int, long	
14	5, 10	N	Int, short	
15			Int, long	
16	5, 10	N	Ext	
17	8, 15	N	Ext	Included in RAM array C

An example layout for the 2, 4 μm FET cell with normal design rules and low resistivity cermet is shown in Fig. 3.1-1. The serpentine resistors dictated the cell size. This size was maintained for the other versions to facilitate arraying the different cells. The layout for 2, 4 μm FETs with normal design rules and a high resistivity film is shown in Fig. 3.1-2. The

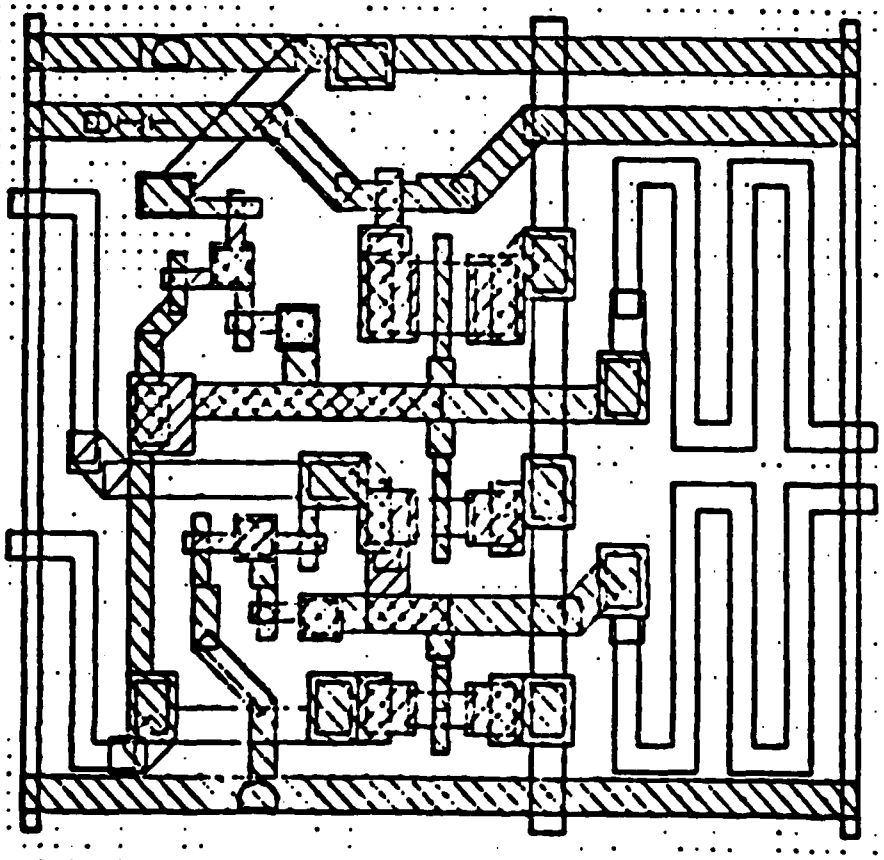


Fig. 3.1-1 RAM cell for low resistivity film, normal design rules, 2 and 4 μm FETs.

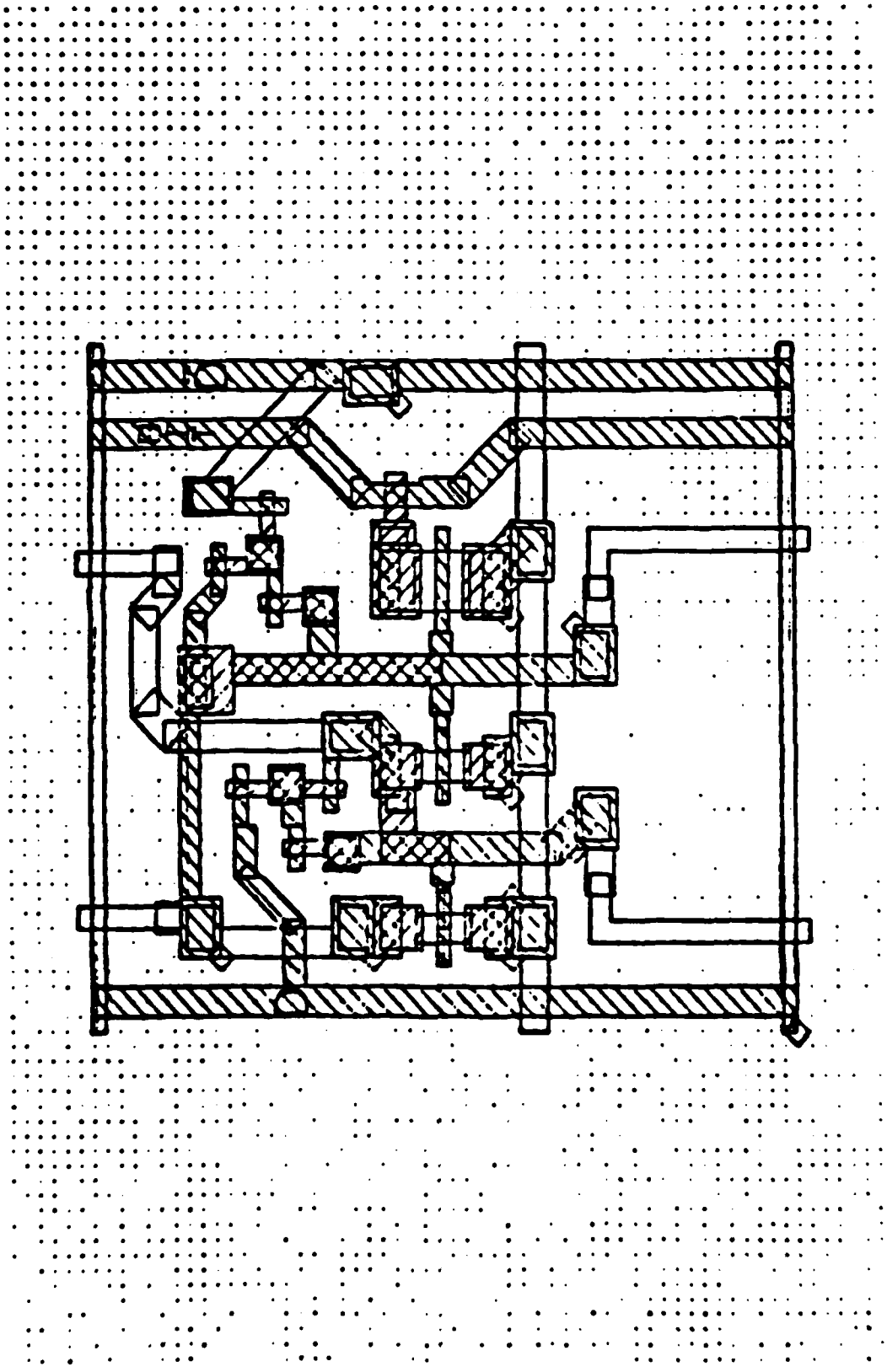


Fig. 3.1-2 RAM cell for high resistivity film, normal design rules, 2 and 4 μm FETs.

difference in the resistors can readily be seen. The spacings of Schottky metal are 2 μm and vias between metal layers are located away from the source or drain regions of the FETs. Figure 3.1-3 shows the same layout with tightened rules where the Schottky metal spacings are 1.5 μm and the vias are located right on the source and drain regions. The idea behind this mask was to avoid the expenditure of extensive layout design time, therefore, no attempt was made to shrink cell size when reduced spacings and smaller components were used in design variations. These cell layout variations are the critical yield and performance determining factors. Once the best design rules are determined and proven, an optimized cell layout will be designed on a later mask set.

Two generic cell layouts were made, one for the cells with larger FETs (5, 10 μm and 3, 6 μm) and one for those with smaller FETs (2, 4 μm and 1, 2 μm). For each of the two, all the variations were made, and a 4 x 8 array formed with the cell design variations scattered through it. For each size, the cell with external resistors appeared only twice; all others appeared either four or five times, a least once in a completely internal location (for evaluation of any proximity effects). The arrangements of RAM arrays A and B are shown in Figs. 3.1-4 and 3.1-5, respectively. The quantity of a given cell variant in these arrays is sufficient for a coarse yield estimate, and good enough to identify and rule out cell designs with very low yield. The two cell designs that were considered "best" and a third very conservative control cell were each arrayed into 4 x 8 RAMs. Tests on these arrays would provide statistical data for preliminary yield analysis.

In addition, alternative current limiting circuits consisting of a FET and one or more diodes were also included on the mask, as well as small FETs for evaluation, diode leakage test patterns, cermet resistor patterns, patterns for alternate resistor fabrication methods, and other process monitor test cells. The organization of mask AP1 is shown in Fig. 3.1-6.

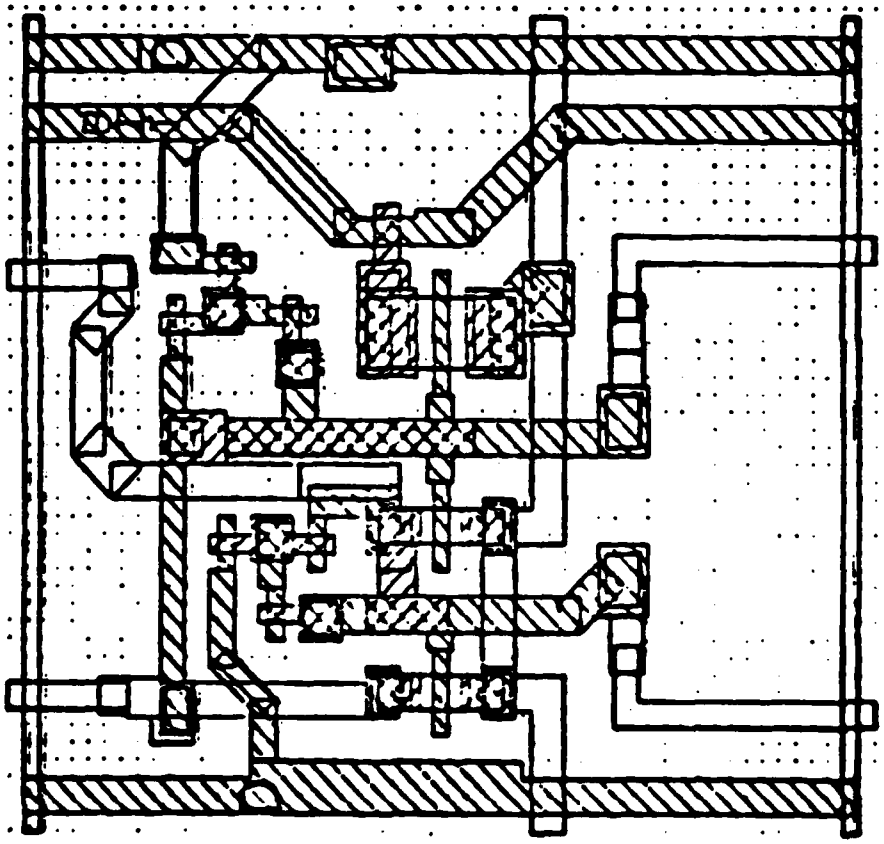


Fig. 3.1-3 RAM cell for high resistivity film, tightened design rules, 2 and 4 μm FETs.

1, 2 μm SHORT R	1, 2 μm SHORT R	2, 4 μm TIGHT RULES SHORT R	2, 4 μm SHORT R
1, 2 μm LONG R	1, 2 μm SHORT R	2, 4 μm TIGHT RULES LONG R	2, 4 μm LONG R
2, 4 μm TIGHT RULES SHORT R	1, 2 μm LONG R	2, 4 μm TIGHT RULES LONG R	2, 4 μm SHORT R
1, 2 μm EXT R	1, 2 μm LONG R	2, 4 μm LONG R	2, 4 μm EXT R
1, 2 μm EXT R	1, 2 μm LONG R	2, 4 μm LONG R	2, 4 μm EXT R
2, 4 μm TIGHT RULES SHORT R	2, 4 μm TIGHT RULES LONG R	2, 4 μm SHORT R	2, 4 μm TIGHT RULES SHORT R
2, 4 μm LONG R	1, 2 μm SHORT R	2, 4 μm LONG R	2, 4 μm TIGHT RULES LONG R
2, 4 μm SHORT R	1, 2 μm SHORT R	2, 4 μm SHORT R	2, 4 μm TIGHT RULES SHORT R

Fig. 3.1.4 RAM array A on mask set AP1.

3, 6 μm SHORT R	3, 6 μm SHORT R	3, 6 μm TIGHT RULES SHORT R	5, 10 μm SHORT R
3, 6 μm LONG R	3, 6 μm SHORT R	3, 6 μm TIGHT RULES LONG R	5, 10 μm LONG R
3, 6 μm TIGHT RULES SHORT R	3, 6 μm LONG R	3, 6 μm TIGHT RULES LONG R	5, 10 μm SHORT R
3, 6 μm EXT R	3, 6 μm LONG R	5, 10 μm LONG R	5, 10 μm EXT R
3, 6 μm EXT R	3, 6 μm LONG R	5, 10 μm LONG R	5, 10 μm EXT R
3, 6 μm TIGHT RULES SHORT R	3, 6 μm TIGHT RULES LONG R	5, 10 μm SHORT R	3, 6 μm TIGHT RULES SHORT R
5, 10 μm LONG R	3, 6 μm SHORT R	5, 10 μm LONG R	3, 6 μm TIGHT RULES LONG R
5, 10 μm SHORT R	3, 6 μm SHORT R	5, 10 μm SHORT R	3, 6 μm TIGHT RULES SHORT R

Fig. 3.1-5 RAM array B on mask set AP1.

<table>
<tr><td>T2</td><td rowspan="2">FAT
FET
(CV)</td><td rowspan="2">FULL ADDER
WITH CORNER
GATE</td><td rowspan="2">RAM
ARRAY
WITH
DAMAGED
RESISTORS</td><td>CURRENT
LIMITERS
1 μ & 2 μ</td><td>CERMET RES
1.0 μ,
DAMAGED R TEST</td></tr>
<tr><td>T1</td><td>CURRENT
LIMITERS
3 μ & 4 μ</td><td>CERMET RES
1.5 μ</td></tr>
<tr><td rowspan="2">FAT
FET
(CV)
MOM</td><td>ELECT. ALIGN.
TEST</td><td colspan="2" rowspan="2">ANALOG GAIN TEST</td><td>CURRENT
LIMITERS
5 μ & 3/4 μ</td><td>CERMET RES
2.0 μ</td></tr>
<tr><td>DYN. RAM
TEST CELL</td><td>FETS
1 μ, 3 μ, 0.75 μ</td><td>DIODE LKGE
TESTS</td></tr>
<tr><td colspan="2">RAM A
RAM CELL VARIETY
WITH SMALLER FETS</td><td colspan="2">RAM B
RAM CELL VARIETY
WITH MEDIUM FETS</td><td colspan="2">RAM C
RAM CELLS
WITH LARGE FETS;
ALSO TIGHT RULES
VERIFICATION CELLS</td></tr>
<tr><td colspan="2">RAM 5
RAM CELL ARRAY
WITH SMALLER FETS,
TIGHT RULES</td><td colspan="2">RAM 8
RAM CELL ARRAY
WITH MEDIUM FETS,
TIGHT RULES</td><td colspan="2">RAM 7
RAM CELL ARRAY
WITH MEDIUM FETS,
NORMAL RULES</td></tr>
</table>

Fig. 3.1-6 Organization of mask set AP1.

3.2 RAM Process Development

Because a low power GaAs RAM cell requires extremely high value load resistors (20-50MΩ), very low threshold FETs (~ 0.5 V) and a high degree of device isolation, additional process development has been required to implement a GaAs RAM technology. Because the control of low threshold voltages was considered to be fairly straightforward, the main processing emphasis for the AP1 mask set was in the development of high value load resistors.

3.2.1 Control of Threshold Voltage and General Wafer Processing

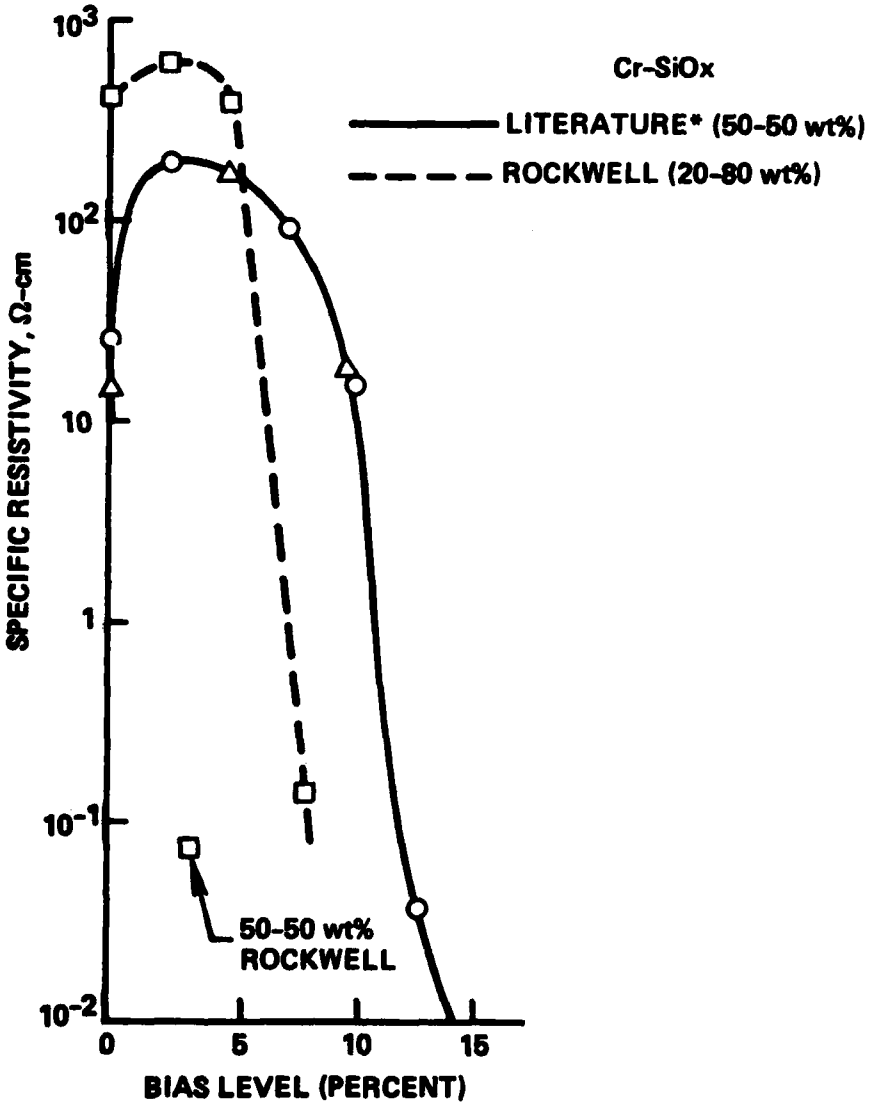
The magnitude of the threshold voltage is one of the most difficult parameters to control because of variations in the shallow, lightly doped n^- layer. The control of this parameter is dependent, not only on the reproducibility and uniformity of the processes which were used, but also on the quality of the GaAs substrates. Typically, the long-range distribution of the FETs from a full GaAs IC wafer are characterized by the threshold voltage of 1.1 V with a standard deviation of 100 mV. Because the RAM cell was designed for subthreshold current operation, threshold voltages of approximately 0.5 V were required. Using the AP1 mask set, implants were systematically varied in order to evaluate proper dose and substrate conditions necessary for V_p = 0.5 V. For a dose of 2.2×10^{12} cm^2 at an energy of 390 keV, the resulting threshold voltage was found to be in the range of 0.85 to 0.95 V, while decreasing the dose to 2.0×10^{12} cm^2 resulted in a threshold voltage in the range of 0.50 to 0.60 V. Thus, the implant conditions of 2.0×10^{12} cm^2 at 390 keV was set as an upper limit for the processing of wafers with reasonable assurance that the proper threshold voltage could be obtained. After the implantation adjustments, processing of the three AP1 wafer lots continued in a normal fashion. Approximately half of the wafers were fabricated without cermet load resistors so that the external resistors could be used to analyze circuit performance. The remaining wafers were processed with cermet films in order to verify resistor processing techniques which would be used on future 256 bit RAM arrays.

3.2.2 High Value Resistor Development

The high value resistor fabrication approach has been to develop thin film cermet ($Cr\text{-}SiO_x$) resistors. A considerable amount of work has been reported[2-4] on cermet resistors, indicating that both acceptable performance and fabrication yield may be achieved with this approach. Cermet resistors, in particular $CR\text{-}SiO_x$, appear attractive since they can be sputter deposited, have high resistivity values, exhibit an acceptable temperature coefficient of resistance, and are compatible with our existing process. In addition, the resistivity can be controlled through the use of bias sputtering[2] and/or oxygen poisoning.[3]

The most desirable method of deposition for cermet resistors is RF sputtering as opposed to flash evaporation (maintains proper composition by completely evaporating all the material from the component source) or co-evaporation (each material is simultaneously evaporated from separate sources) techniques. Sputtering provides a more reproducible thin film composition since the sputtering target is composed of a preselected metal-insulator composition ratio. Also, the thickness step coverage and uniformity control resulting from sputtering is superior to evaporation techniques.

The initial work with cermet film deposition was carried out following the guidelines of Ref. 2. The $Cr\text{-}SiO_x$ films were deposited on dielectric coated silicon substrates. For the preliminary runs, SiO_2 was the dielectric material, while for the later runs in which resistor test patterns were fabricated, plasma deposited silicon nitride (PSN) was used. The depositions were carried out in a conventional RF sputtering system using a 15 cm diameter target. Two different target compositions were tested in an effort to determine the proper resistivity range; the first target consisted of 50-50 wt% Cr-SiO, while the second consisted of 20-80 wt% Cr-SiO. For all depositions, the argon sputtering pressure was maintained in the range of 4-10 μm while the target voltage was constant at 2000 V. As expected, the film resistivity, as measured by a four point probe, was found to vary both with substrate bias and target composition. Typical results are shown in Fig. 3.2-1. Since the re—



*IBM J. RES. DEV.

Fig. 3.2-1 Comparison of cermet resistivity uding different sputter target compositions.

sistivity of the 50-50 target was found to well below the desired values of 200-500 Ω-cm, some preliminary attempts were made to increase the resistivity by oxygen poisoning. However, these techniques were found to be highly non-reproducible and were abandoned in favor of different target composition. The best results were obtained with the 80-20 target and a grounded substrate (0 bias). It was also found that the resistivity was sensitive to the argon sputtering pressure, and thus proved an additional means for "fine tuning" to the desired resistivity value.

Since it was initially proposed that cermet resistors could be trimmed by ion milling, it was of interest to experiment with the change in resistivity as a function of film thickness. Two films were deposited, one at 0 bias level and the other at 2.5% bias level with an initial thickness of 5600A and 6000A, respectively. These films were then ion milled for a specific time in order to reduce the film thickness. A new thickness was determined and the resistivity measured using the four point probe technique. The results are shown in Fig. 3.2-2. The dashed lines represent the values expected of constant bulk or specific resistivity vs thicknesses calculated from the initial film resistivity and thickness, while the data points are the result obtained from the experimental runs. The films exhibit thickness vs resistivity in the anticipated manner, indicating that films in the range of 3000A should be sufficient for RAM applications.

The process which was pursued for the implementation of cermet thin film resistors for the AP1 RAM cell is shown schematically in Fig. 3.2-3. Basically, the appropriate thickness and resistivity of cermet material is deposited on second-level dielectric and the resistors are defined by ion milling. After etching via windows, the second-level metal is deposited with the interconnects also defined by ion milling. At this point, the resistors can be probed and adjusted (trimmed) in value, if necessary, by thinning with additional ion milling. Additional variations to the process included both thermally stabilizing the cermet resistors and protecting the resistors with a final dielectric layer. Although this process provided a good first effort

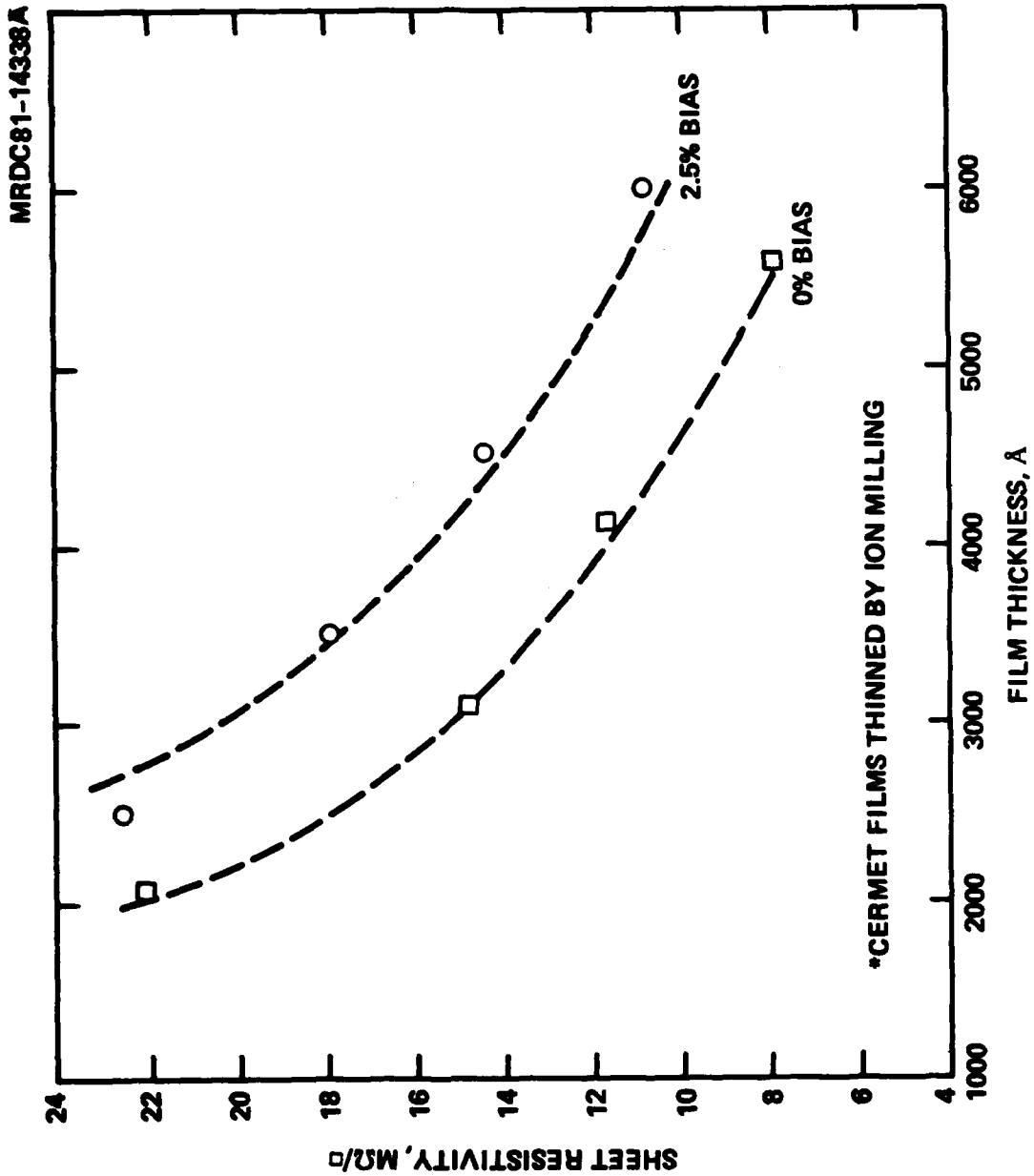
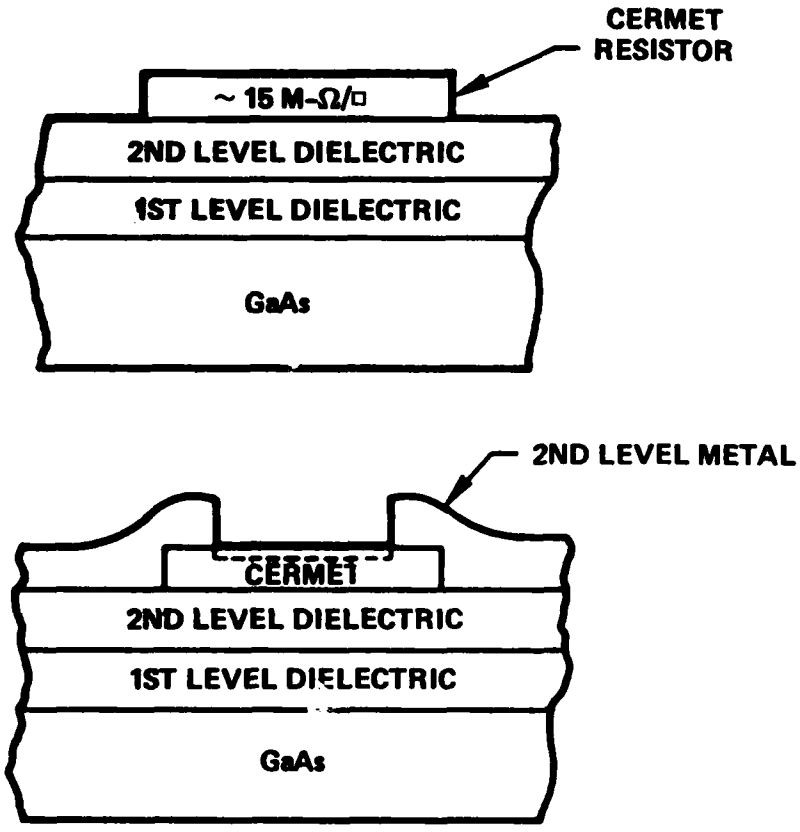


Fig. 3.2-2 Cermet sheet resistivity as a function of film thickness.



FOLLOWING 2ND LEVEL DIELECTRIC:

1. DEPOSIT CERMET FILM
2. MASK CERMET RESISTOR
3. ION MILL RESISTOR
4. MASK VIAS
5. ETCH VIAS
6. DEPOSIT 2ND LEVEL METAL
7. MASK 2ND LEVEL METAL
8. ION MILL 2ND LEVEL METAL
9. SINTER CERMET CONTACT

Fig. 3.2-3 Cermet resistor process steps.

result for the initial RAM cells, later measurements shows a nonuniformity in contacting second-level metal. As a result, a minor modification was made to this basic process before beginning to fabricate 256 bit arrays. The cermet processing technique for these arrays is discussed in Sec. 4.2.

3.3 RAM Cell Test Results

The testing procedures for the AP1 mask set concentrated on an evaluation of active devices and individual RAM cells. In addition, a preliminary evaluation of radiation effects on device performance was also performed. The RAM cell tests were conducted primarily with external load resistors, since the cermet process continued to be developed during this time.

3.3.1 Device and RAM Cell Performance

Diodes are used in GaAs circuits for voltage level shifting. For appreciable current densities, the forward voltage drop across a diode is normally ≈ 0.7 V. In the RAM-compatible lower current range, the voltage drop is much lower. The I-V characteristics of level shifting diodes were measured on 10 parallel 1 μm x 1 μm diodes as shown in Fig. 3.3-1. The measurement result indicates that in the current range of tens to hundreds of nanoamperes, the voltage drop across one diode ranges between 0.45 V and 0.52 V (instead of 0.7 V). In this measurement, it was also found that the characteristics of doubly implanted diodes were subject to more variability and higher dark currents than were those of singly implanted diodes. Therefore, singly implanted diodes were chosen in the following RAM cell designs.

The FETs in a RAM cell are operated in the threshold conduction region in which the operating characteristic departs from the square law $I = K(V_{gs}-V_T)^2$. Measurements of the low current characteristics of 2 μm switching FETs shown in Fig. 3.3-2. In Fig. 3.3-2, the subthreshold conduction of these FETs can be represented as $I = I_0\exp(-\alpha qV_{gs}/kT)$, instead of square law. It can also be seen from this measurement that to decrease the current by one decade requires a change in V_{gs} of approximately 150 mV. This figure can serve

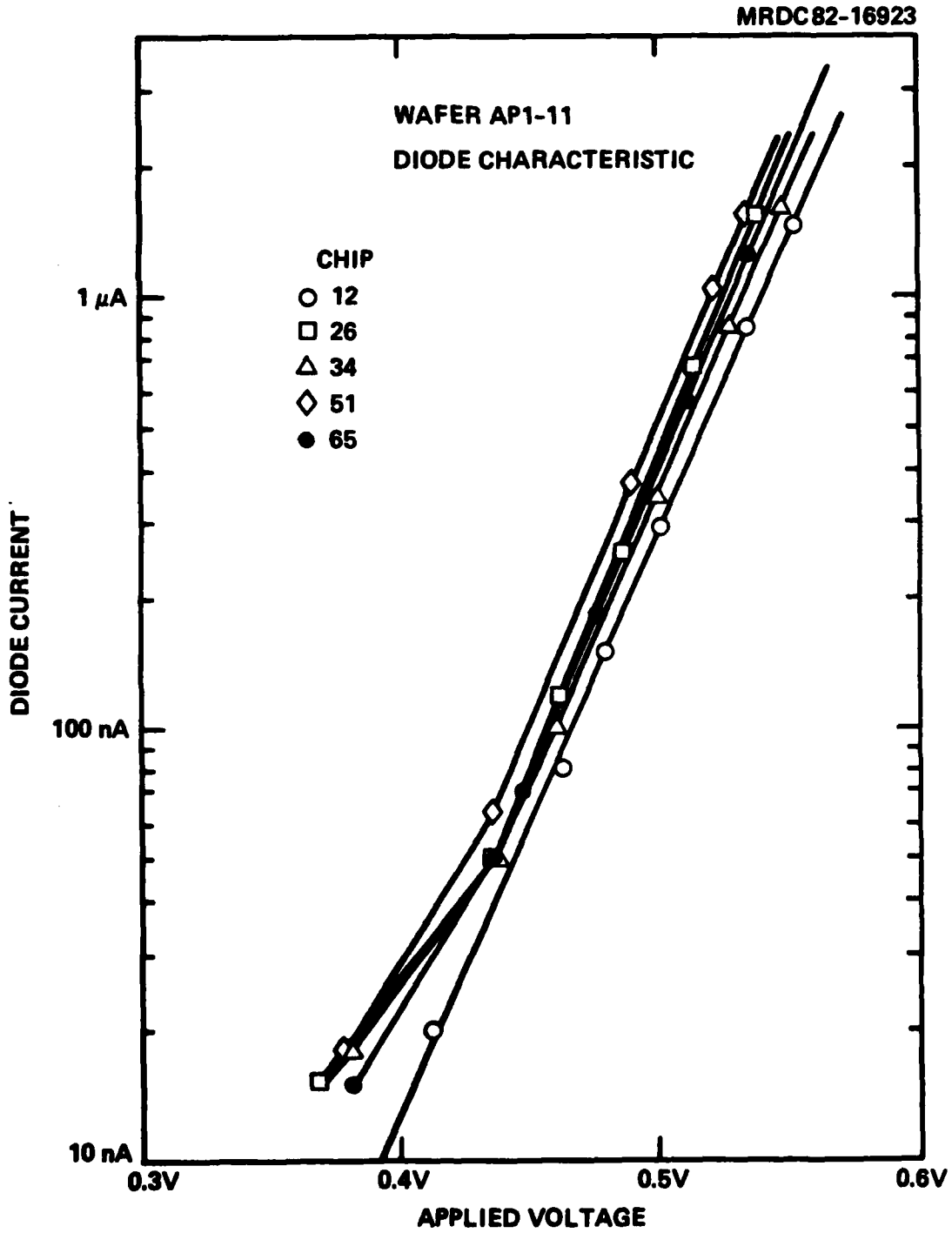


Fig. 3.3-1 Wafer AP1-11 diode characteristic.

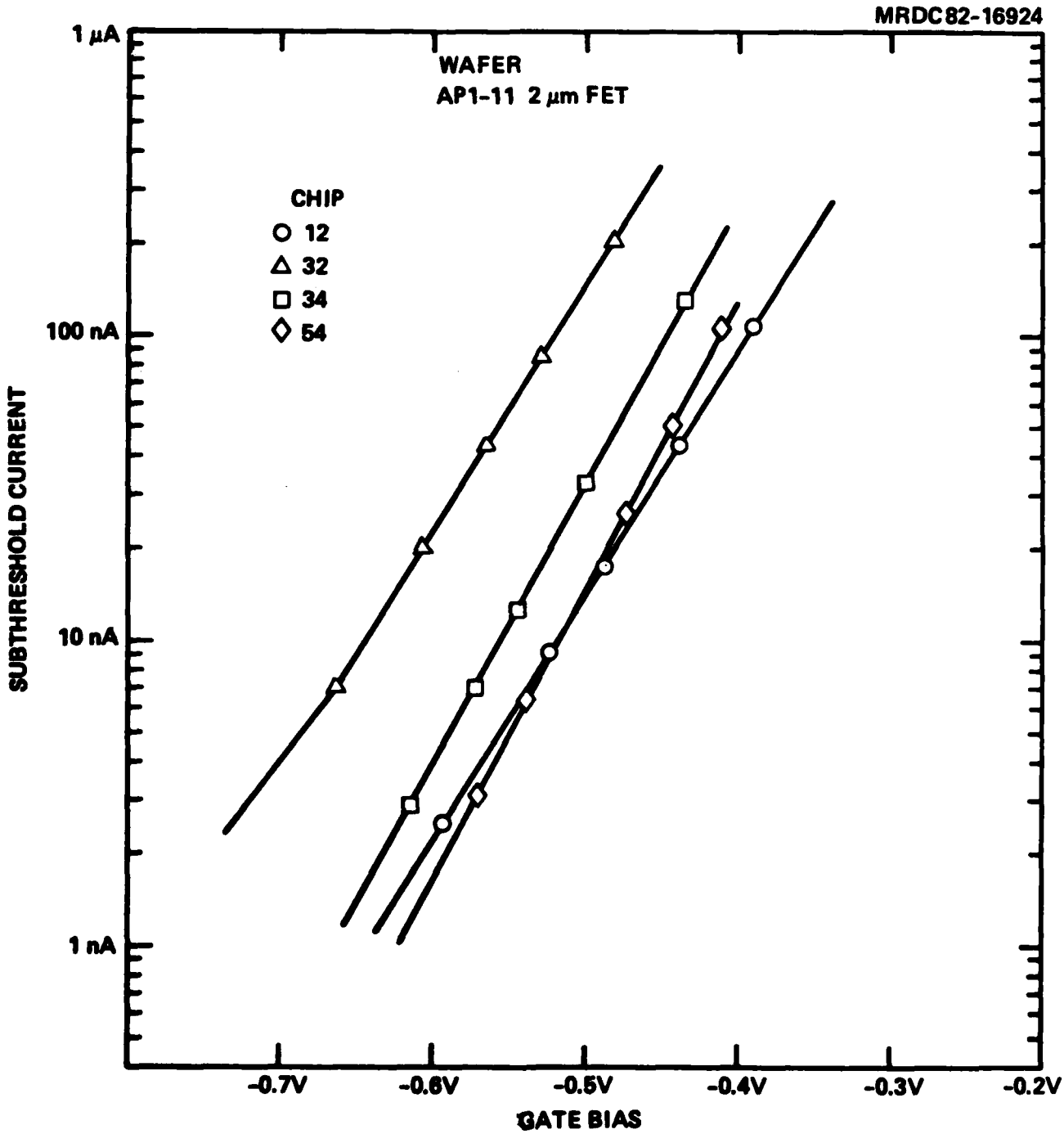


Fig. 3.3-2 Subthreshold conduction of FET.

as a design guide in defining the low current turnoff voltage of a FET. For example, if low current turnoff is defined as one order of magnitude decrease in current, it can be taken as a voltage magnitude 0.15 V greater than the nominal pinchoff voltage. The measurement results shown in Fig. 3.3-1 and 3.3-2 provide a preliminary set of design parameters, and verify the viability of RAM cell operation in the 10 to 100 nanoampere range with regard to current leakage margins and device behavior.

Testing procedures for cell operation included plotting output voltage as a function of the negative supply voltage, V_{SS}, with a fixed V_{DD} and word line voltage ($V_{word\ line}$). when V_{SS} is increased negatively from 0, with $V_{word\ line} = 0$, the curves of Fig. 3.3-3 result. With V_{SS} near 0 V, both latch FETs and the output FET are on, the voltages at the drains of the latch FETs are 0 V, and the output voltage is one diode drop above ground ($\approx$ 0.6 V). As the magnitude of V_{SS} is increased, the gates of the transistors become negatively biased, current flow is limited, and the output voltage rises. The situation is that of a balanced amplifier. Further increases in V_{SS} bring the gate voltage to $V_{pinchoff}$, at which point the circuit becomes bistable; the output will be high or low depending on the state of the latch circuit. $|V_{SS}|$ can now be increased over a considerable range with bistable operation maintained. Eventually, it becomes so negative that the "on" FET has its current reduced to where it will not clamp the drain voltage to 0 V which starts to rise. Near this point, the circuit loses its bistability as the voltage on the drain of the "on" FET rises and no longer holds the gate of the "off" FET below pinchoff. This gives the margin of operation for V_{SS} with a given V_{DD}, and with $V_{word\ line} = 0$; the margin is wider for higher values of V_{DD}.

The disabling characteristic of the cell can be determined by repeating the test described above, with $V_{word\ line}$ set at various voltages as shown in Fig. 3.3-4. As $V_{word\ line}$ approaches the full disabling voltage of 1.5 V, the distinction apparent in the output between a "1" and a "0" disappears and the range of V_{SS} for bistability decreases. The curves in Fig. 3.4-4 are measured data for a specific circuit with 2 and 4 μm FETs and tight design rules.

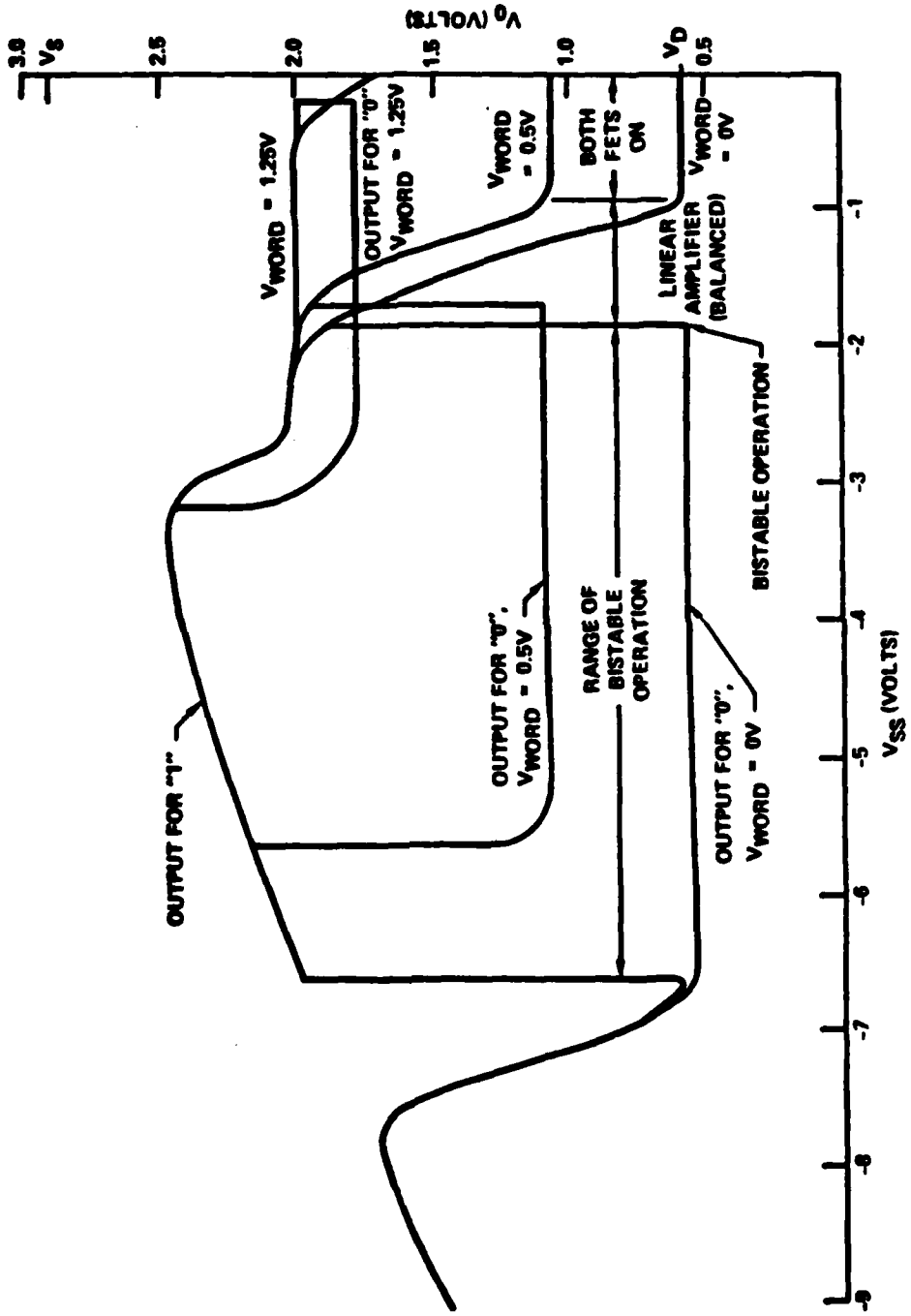


Fig. 3.3-3 Operation region for RAM cell.

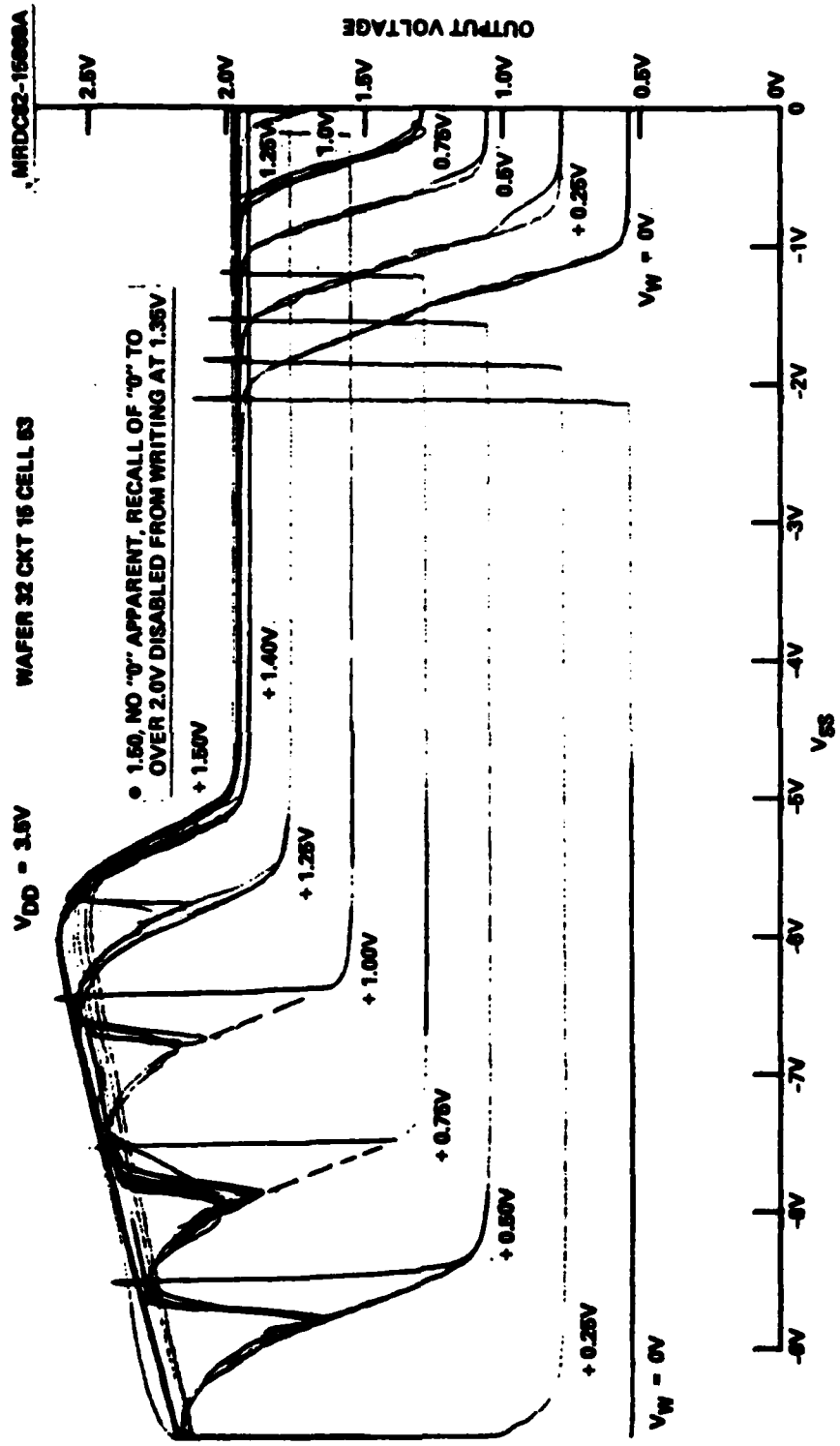


Fig. 3.3-4 Disabling characteristic of a RAM cell.

The effect of V_{DD} variations on the operating window are shown in Fig. 3.3-5. In this measurement, a very high value of sense voltage on the output was used; any output voltage above approximately 2.0 V is to be regarded as a "1", and the remaining structure of the figure (above 2.0 V) to be ignored, since in an array the output voltage would be clamped. The predominant effect of 0.5 V change in V_{DD} is to produce an approximate 1.0 V widening of the operating region for the stored "0" (the lower part of the loop) with respect to V_{SS}; the widening takes place in the high V_{SS} end with almost no change in the low V_{SS} end. From these data, it can be concluded that the cell is not particularly sensitive to V_{DD} variations.

The effect of resistor variation on the cell operating window was also verified experimentally. For a cell with external resistors, the values were set at nominal the the operating window plotted as shown in Fig. 3.3-6. then, in turn, the pullup resistor was increased by 10%, the pulldown resistor was increased by 10%, and finally both resistors were increased by 10%. As would be expected, since the circuit operation depends on the ratio of the resistors more than absolute value, increasing both had little effect. Increasing the pulldown resistor increased the window, while increasing the pullup resistor decreased it, but not by large amounts. These data show that the cell design is not critically dependent on resistor values.

Some of the above data (e.g., resistor variation and word line voltage effects) were taken at lower values of V_{DD} (3.5 V or 2.5 V). There were two reasons for this: one is that the variation under study was more pronounced (i.e., caused a larger percentage variation with espect to V_{SS}) at lower values of V_{DD}, so testing at lower value of V_{DD} was done to aid analysis of circuit operation by accentuating the effect. The second reason was to cause the left-hand portion of the operating window to occur at magnitudes of V_{SS} safely below the breakdown voltage of the circuit. All of the effects studied scaled to higher voltages without essential change, except a decrease in the percentage variation relative to V_{SS}.

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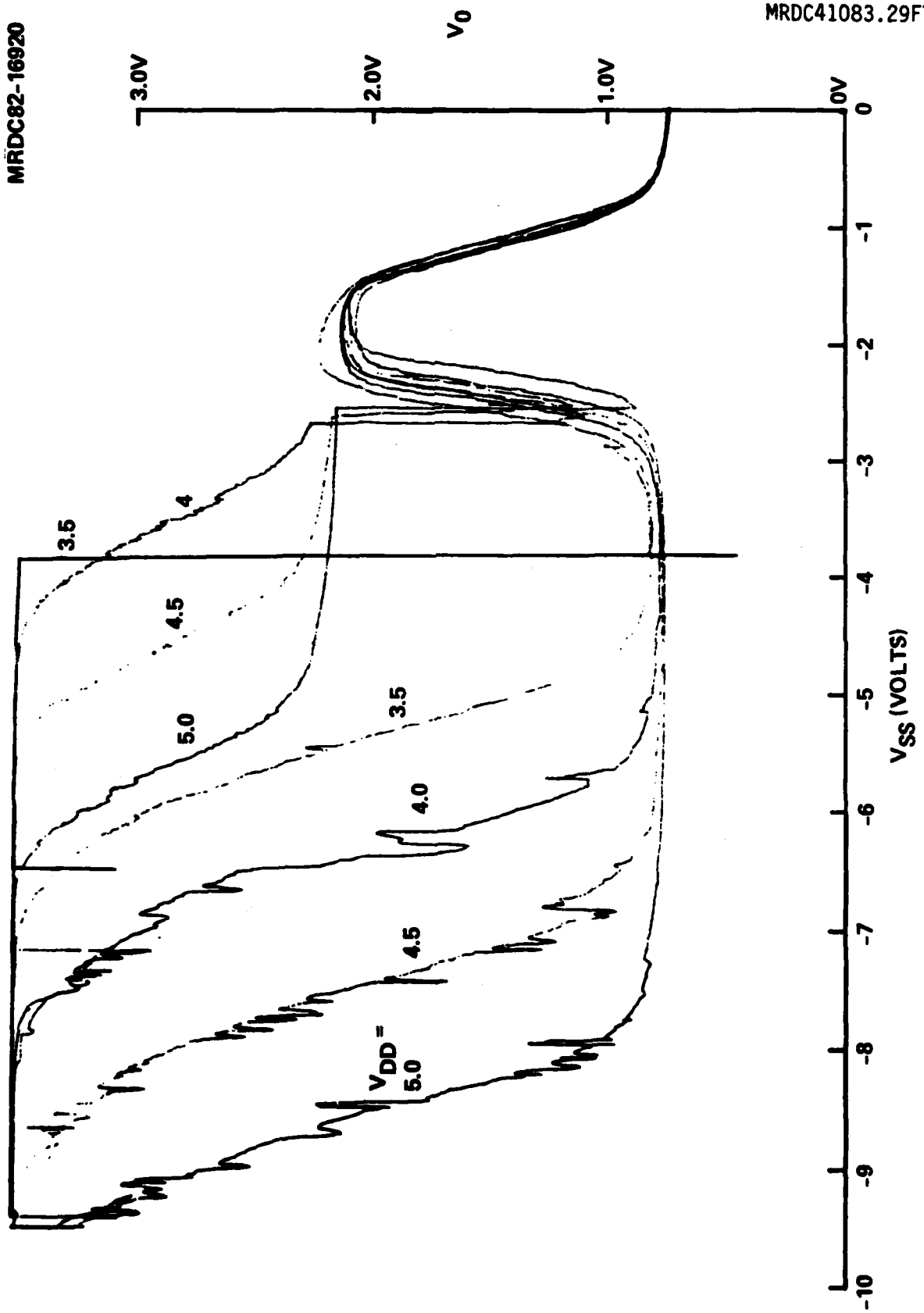

Fig. 3.3-5 Effect of V_{DD} variations on cell operation.

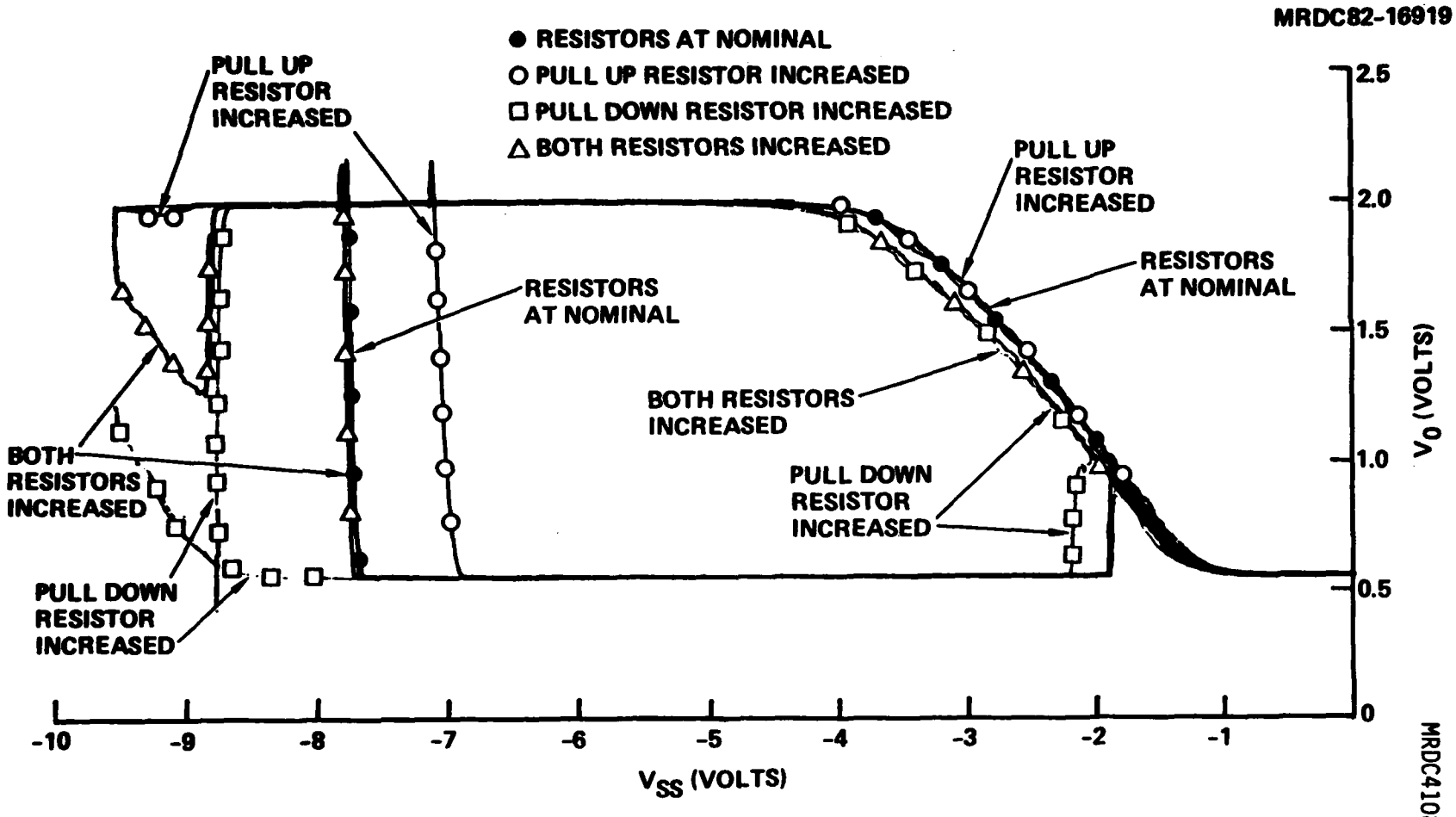

Fig. 3.3-6 Effect of 10% resistor variations on cell operation measured on a cell with external resistors.

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Dynamic testing of the cell was also performed. As the word line voltage, V_W, in increased, the point is reached where a write pulse on the appropriate line does not change the state of the cell; the cell is then disabled. Disabling occurs for $V_W \approx 1.3$ V. As the word line voltage reaches 1.5 V, the output voltage is essentially the same for a stored "0" or a "1", i.e., the operating loop traced out as V_{SS} is varied reduces to a line (or single curve). When V_W is again lowered, the voltage is appropriate to the stored state, however. If V_W is raised high enough, then subsequently lowered, the output voltage will always be that for a "1", regardless of the original state; the cell is "forgetting" data. The word line voltage V_W for forgetting is greater than 2 V for all cells tested with $V_{DD} = 3.5$ V. For $V_{DD} = 5$ V, the forgetting voltage was $V_W \approx 2.4$-2.5 V.

One important parameter influencing memory cycle times is the minimum pulse width that can write or change the state of a cell. In dynamic testing, cells wrote "1" or "0" reliably and consistently with 2 ns pulses (the lower limit of the pulse generator). The cell design is, therefore, more than fast enough for a 10 ns access time RAM.

3.3.2 Radiation Tests

Total dose radiation experiments were carried out using one of the wafers from the first mask set, AP1-11. This wafer was irradiated with a total gamma dose of 10^7 rad, and the following parameters wre measured before and after irradiation: 1) the substrate leakage current, 2) the subthreshold conduction of the FETs, and 3) the I-V characteristics of the diodes. With the exception of a slight change in diode forward voltage drop, no change in characteristics occurred due to radiation exposure. Test results from wafer AP1-11 are described in detail below:

Substrate Leakage Current - The substrate leakage current was evaluated by measuring the I-V characteristics of the isolation test pattern. This pattern was 50 μm wide with a 3 μm gap between the two n^+ implants. The negligible decrease in substrate current, as shown in

Fig. 3.3-7, demonstrates that the isolation properties of the GaAs substrates are unaltered by irradiation.

Subthreshold Characteristics - The subthreshold characteristics of a small FET (gate dimensions 24 μm wide by 1 μm long) before and after irradiation are shown in Fig. 3.3-8. The slight shift in the log I vs V_{gs} curve represents a decrease in the magnitude of the effective threshold voltage of approximately 15 mV. It is noteworthy that the slope of the curves in the low current region does not change. Gate leakage current was less than the measurement sensitivity during both tests. The conclusion is that 10^7 rads caused no significant change in FET subthreshold characteristics, the slight actual change observed being in a direction to improve circuit operation.

Schottky Diode Characteristics - The Schottky diode characteristics before and after irradiation are shown in Fig. 3.3-9. The ideal characteristic of the Schottky junction remains unchanged after irradiation, as indicated by the linear relation of the log I vs V curve. The most notable change is a decrease in barrier height of approximately 70 mV, as well as a small increase in the ideality factor, n. The lower barrier height causes an upward shift in the log I vs V curve, and therefore a reduction in the forward voltage drops across the diode at a given current. The magnitude of the change is approximately 50 mV for currents in the tens of nanoamperes. In the case of the RAM cell, the decrease in forward voltage tightens the design restrictions, but it should be partly compensated by the accompanying slight decrease in FET threshold voltage. These preliminary test results are indicative of the smll magnitude of radiation effets. The small voltage shift occurring in the diodes can be accounted for in the design of the circuit and, therefore, should not be a problem.

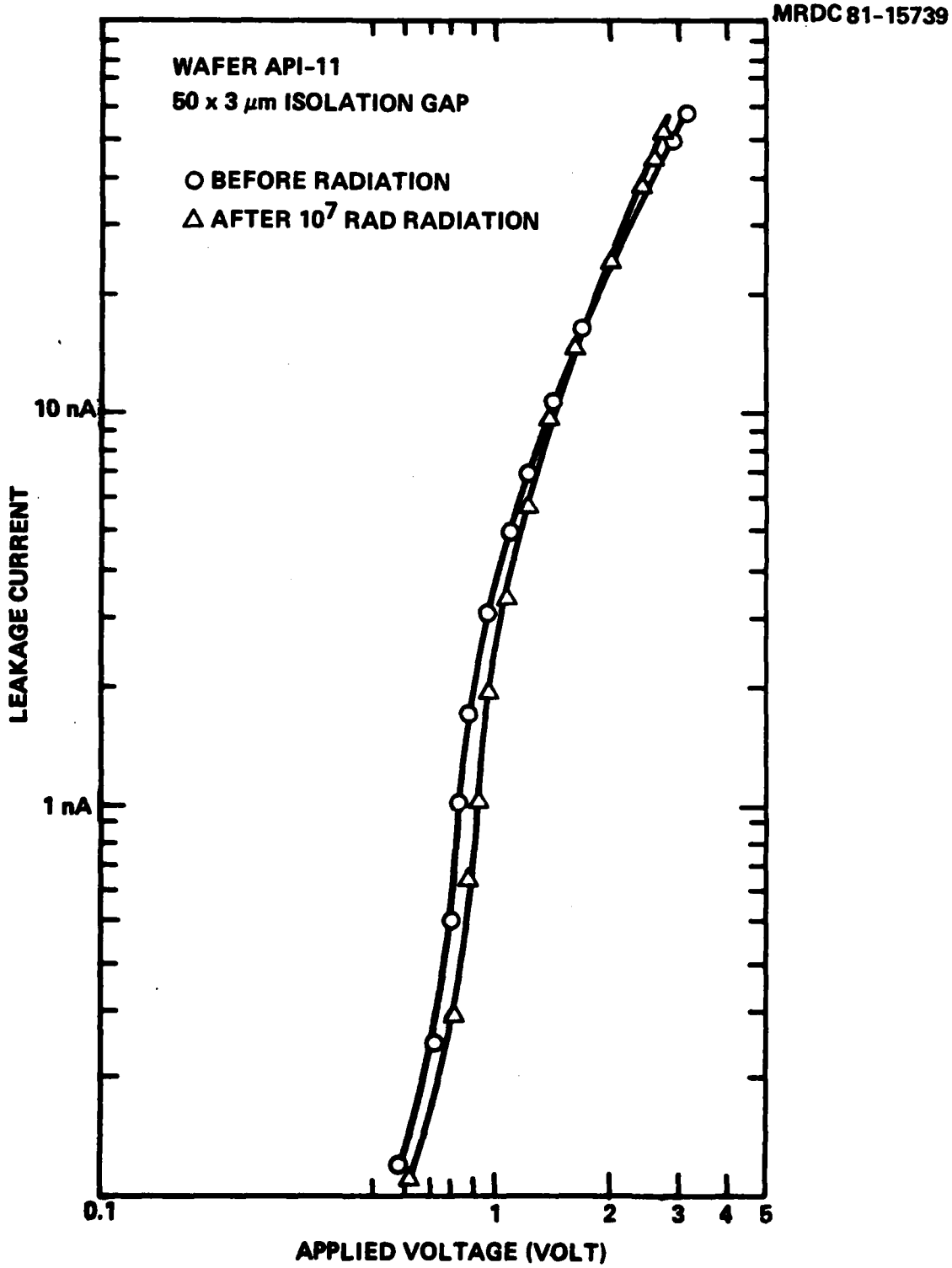

Fig. 3.3-7 Substrate leakage measurements.

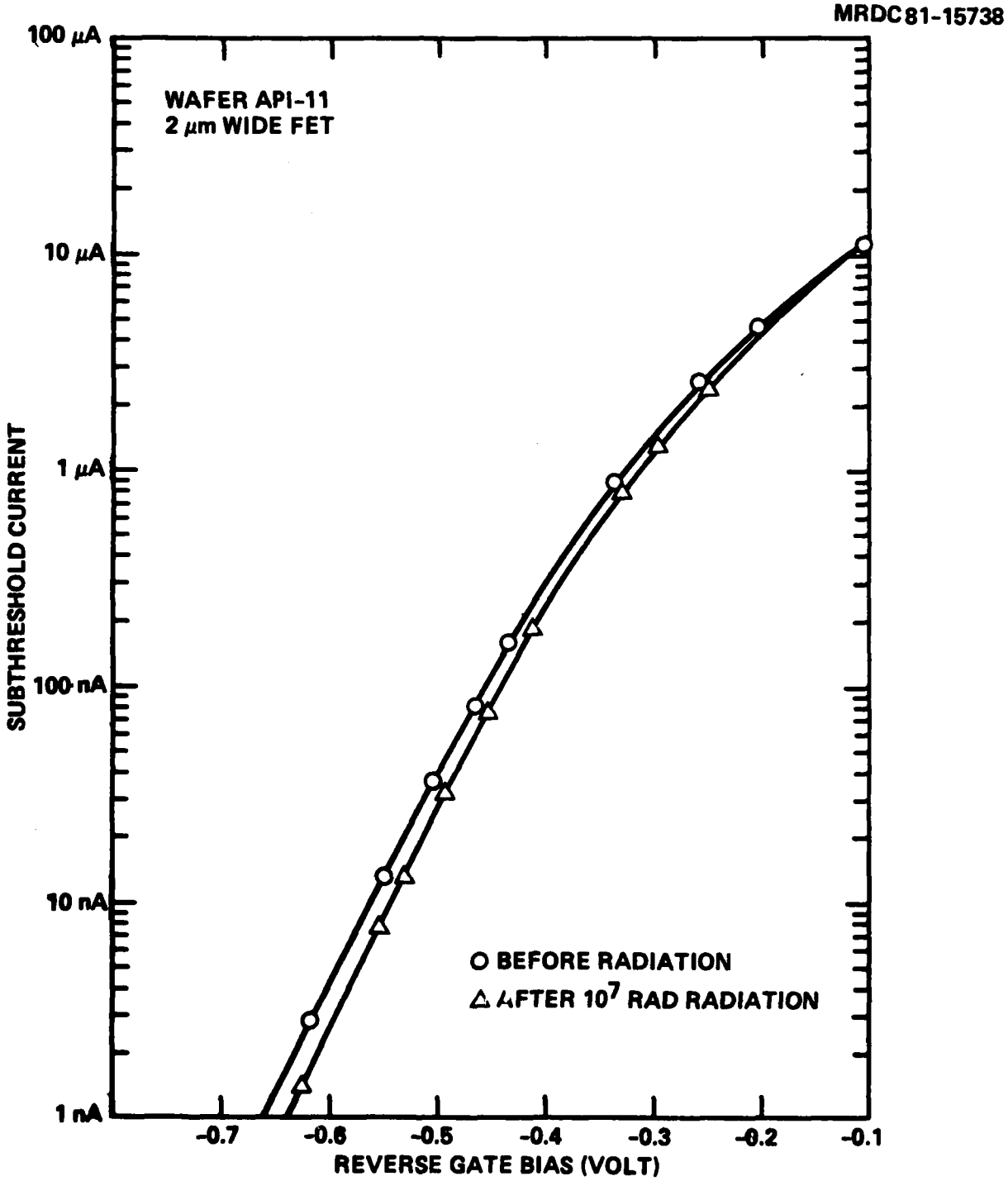

Fig. 3.3-8 Variation of subthreshold current with radiation.

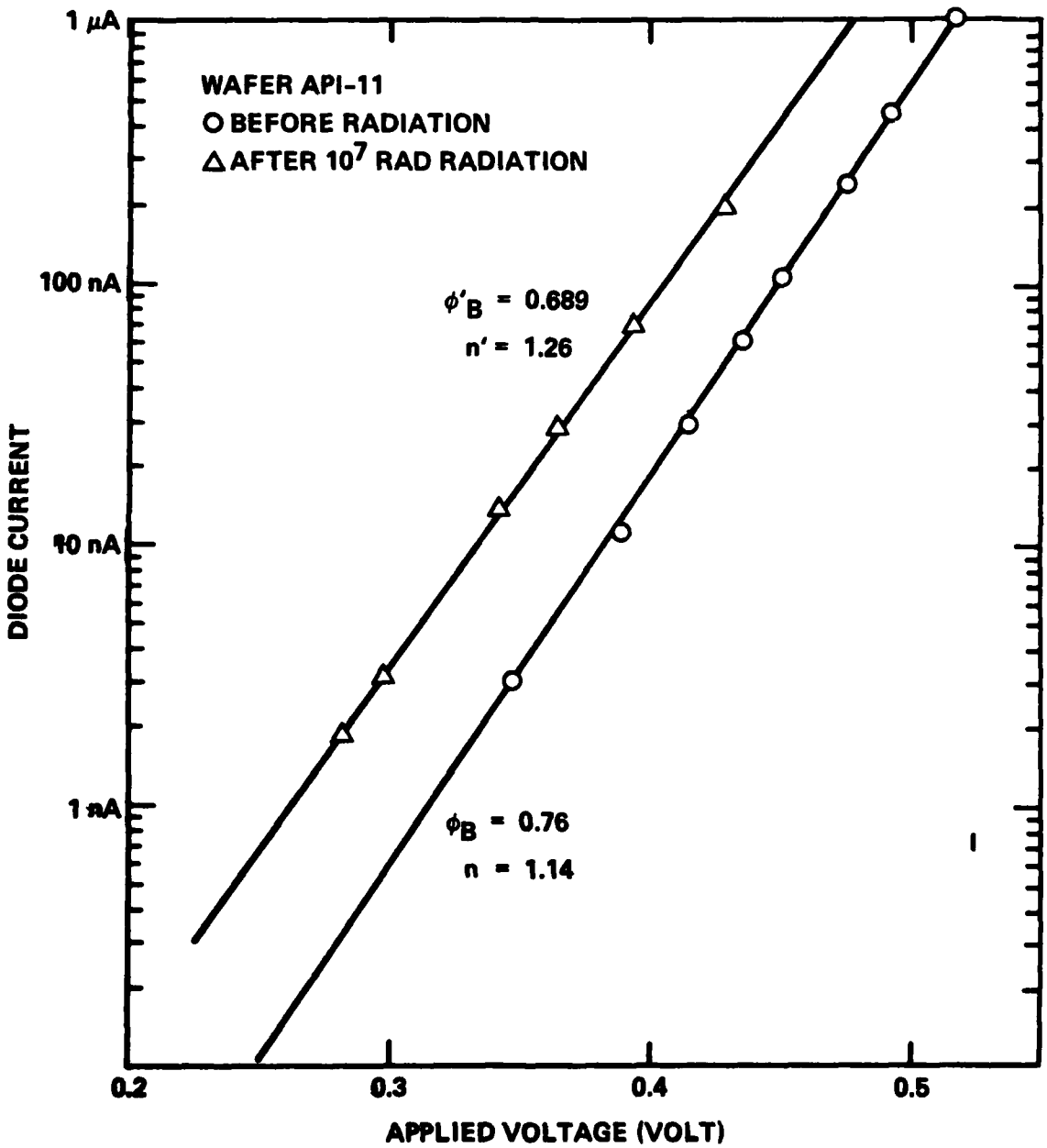

Fig. 3.3-9 Diode characteristics before and after radiation.

A number of other device parameters, such as FET threshold voltage, saturation current, and K value also show a slight, but unimportant change after irradiation of 10^7 rads. Table 3.3-1 shows the average value and the standard deviation for these parameters, both before and after irradiation. The slight decrease in the saturation current, I_{DSS}, after irradiation is not expected to effect the operation of the RAM cell which operates at current levels much lower than I_{DSS}. A fully functional RAM cell was also tested dynamically before and after irradiation; oscillograms of multi-function operation are shown in Fig. 3.3-10a and b. The data output shows writing "1", writing "0", and remembering both "0" and "1" when re-enabled afer being disabled. The same voltages were applied in both cases. The absence of any apparent change indicates that cell operation is insensitive to the slight shift in the characteristics of the devices caused by irradiation of 10^7 rads.

Table 3.3-1

50 μm x 1 μm Gate FET

Variation in Threshold Voltage, Saturation Current, and K Value Before and After 10^7 rads. The Following Data is the Average of 35 FETs

	$-V_p$ (volts)	σV_p (volts)	I_{DSS}	σI_{DSS}	K (ma/V^2)	σ_K (ma/V^2)
Before Radiation	0.493	0.100	0.800	0.264	3.395	0.366
Before Radiation	0.504	0.100	0.787	0.258	3.149	0.300

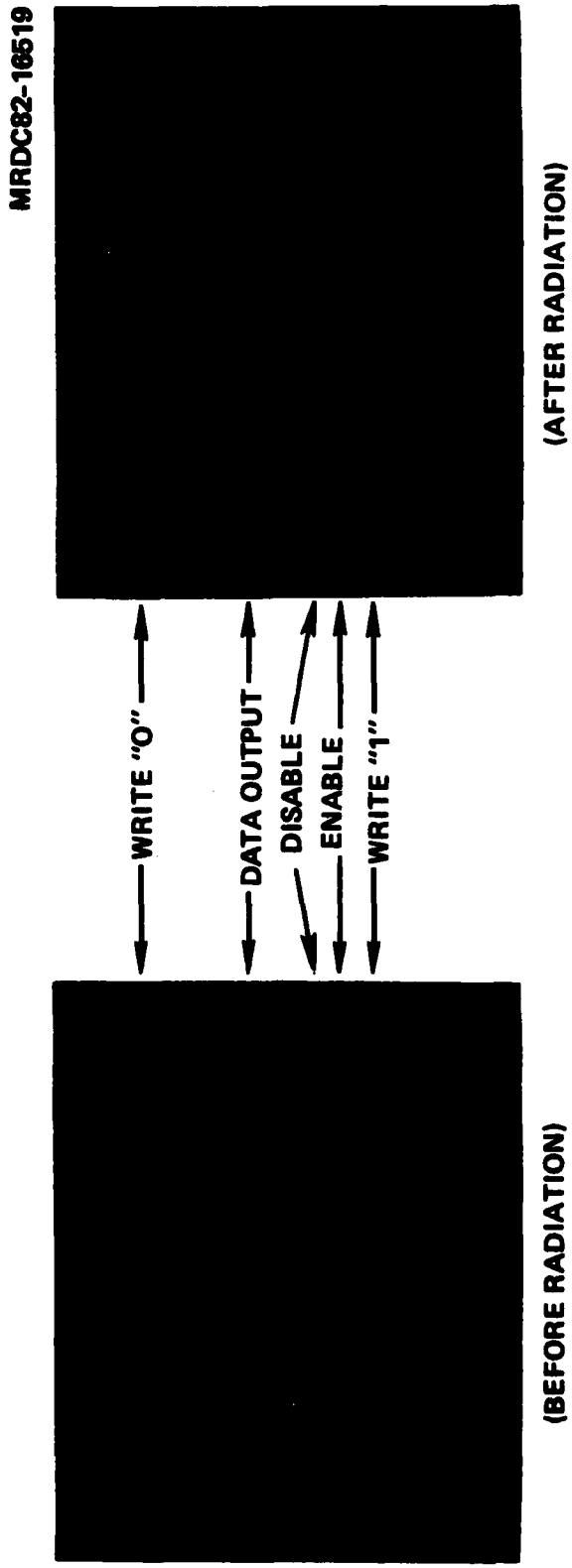

Fig. 3.3-10 Fully functional RAM cell after total dose radiation of 10^7 rad.

4.0 RM2 MASK SET

The AP1 mask fabrication and testing characterized the levels of diode voltage drop as a function of current, defined the minimum allowable threshold voltage for cell operation, and provided information on cell design and layout trade-offs relative to yield. These results provided a sound basis for the design, fabrication and testing of a 256 bit RAM array.

4.1 RM2 Design Approach and Layout

The design approach taken for the second mask set RM2 primarily focused on collecting yield statistics, and was somewhat less concerned with achieving the 1.0 μW/bit power level. A notable change in the cell design of RM2 was to increase the current level in the diodes from 10 nA to 40 nA, allowing cells with slightly higher more negative threshold voltage FETs to be used. This change eased the design task of the decoder circuits that were to be included for the first time in this mask set. The baseline RAM cell for the 256 bit RM2 mask was designed for a 1.8 μW/bit power level; the layout is shown in Fig. 4.1-1. Preliminary circuit designs were also made for the decoder circuit, shown in Fig. 4.1-2.

Arrays with variations on cell design directed toward operation with more negative threshold voltages were also included. Three 256 bit arrays, in all, with decoders were included. These were (as shown in Table 4.1-1): 1) the baseline low power cell (40 nA in diodes), 2) a high power version with four times the current level (160 nA in diodes), and 3) a low current version with three diodes (40 nA in diodes). Another array (with baseline cells) without decoders was also included for direct probing. Due to pad count and layout limitations, the size of this array actually was 14 x 16 = 224 rather than the full 16 x 16 = 256; the 224 size is sufficiently close to 256 that it virtually does not affect the yield study. The RM2 mask organization is shown in Fig. 4.1-3 with the layout shown in Fig. 4.1-4.

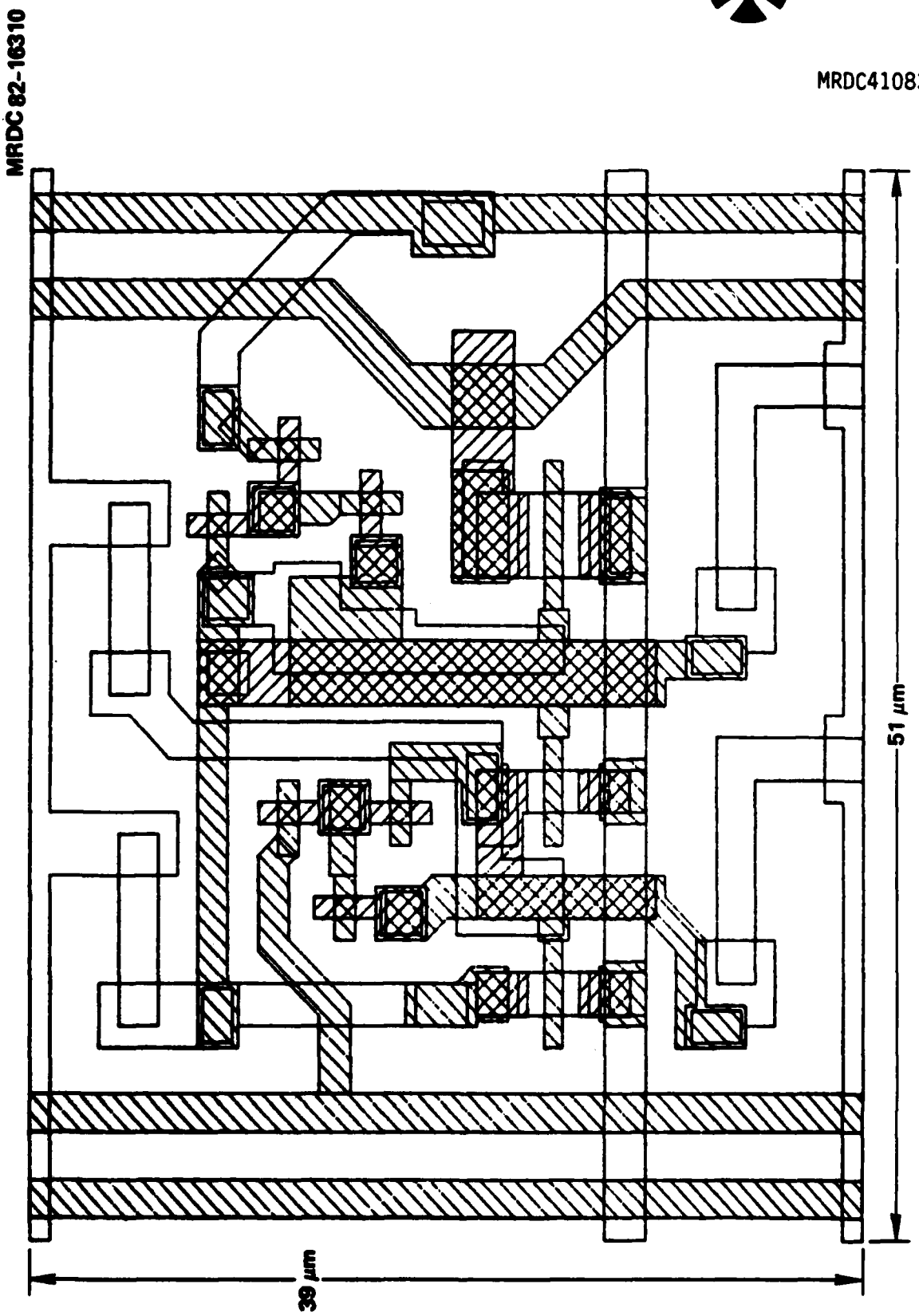

Fig. 4.1-1 GaAs static RAM cell.

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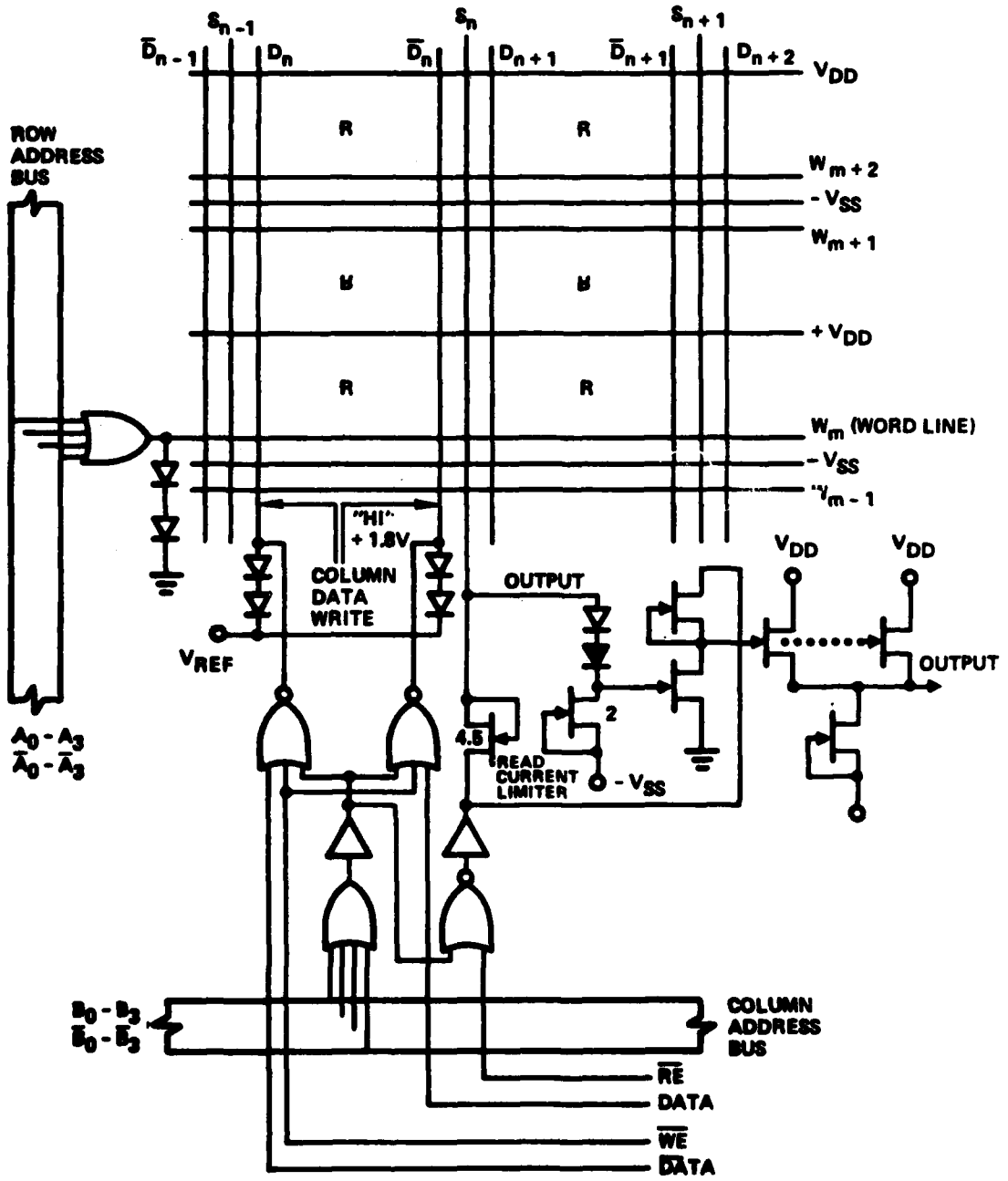

Fig. 4.1-2 Peripheral circuits for 256 bit static RAM (RM2).

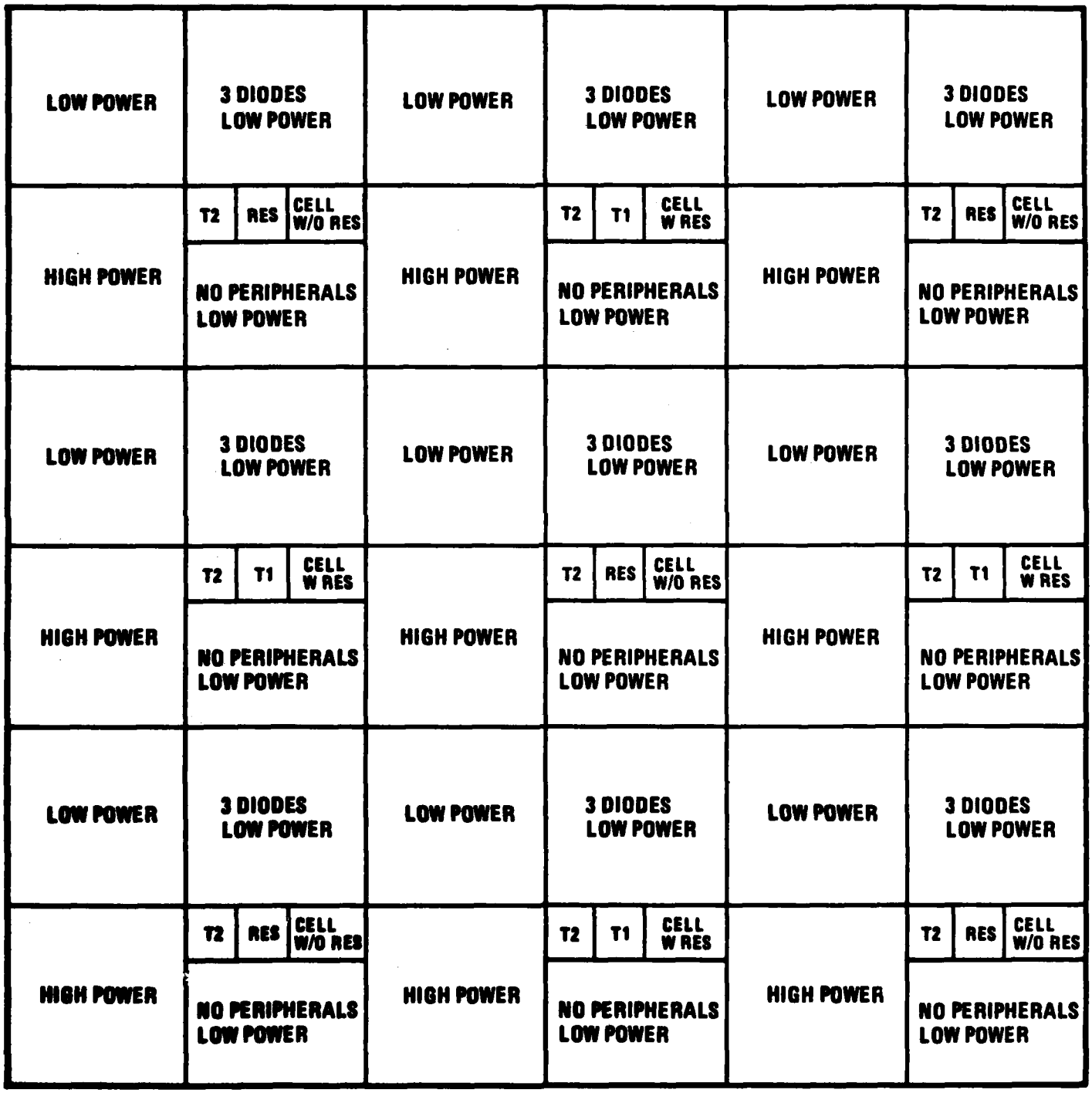

Fig. 4.1-3 256 bit GaAs RAM mask (RM2).

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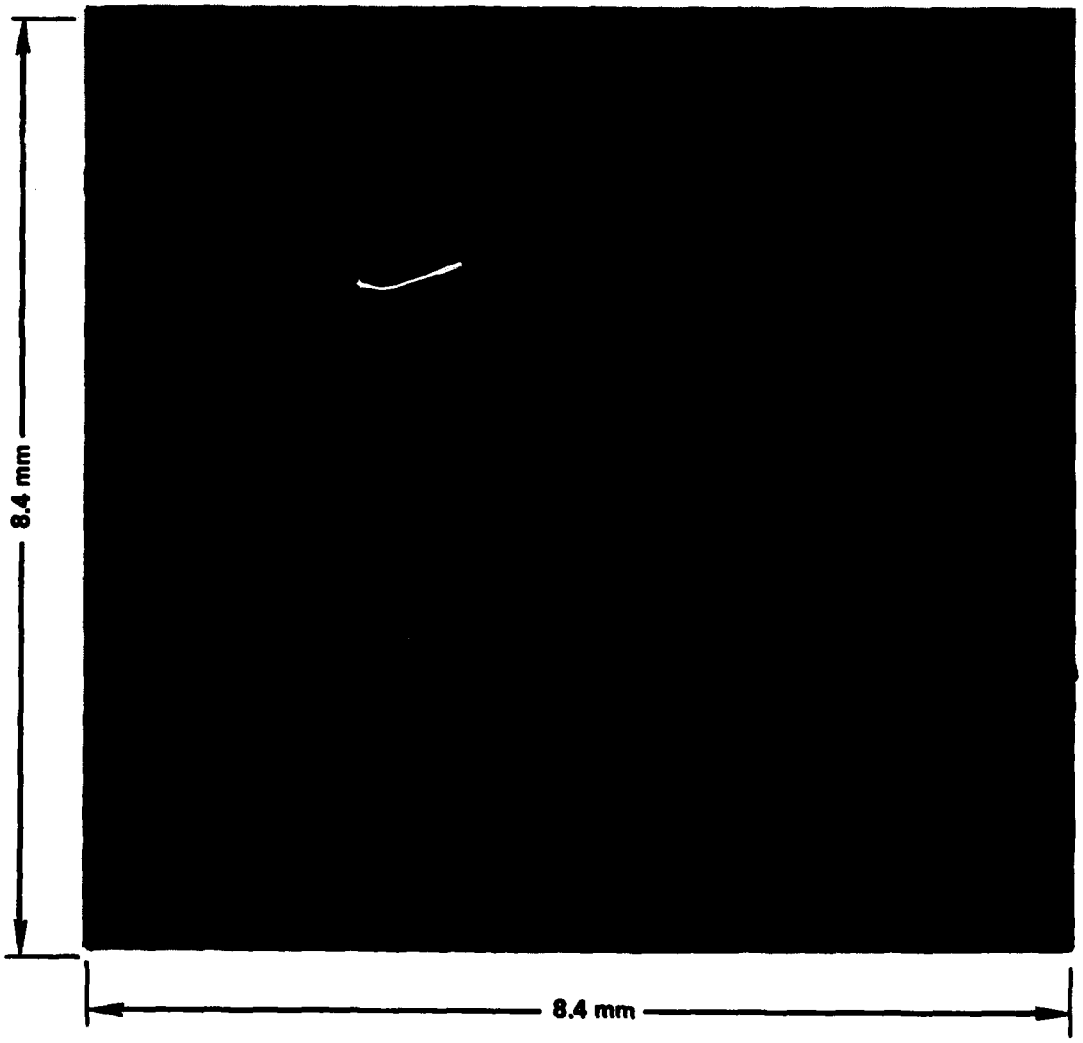

Fig. 4.1.4 256 bit GaAs RAM mask (RM2).

Table 4.1-1

RM2 Mask Set
Three Versions of RAM Cell

1. Low Power (Standard Version)

   - 22 and 50 megohm resistors
   - Power per cell: 2.3 μW enabled, 1.8 μW disabled

2. High Power (will work with higher pinchoff voltages, but at higher power)

   - 6 and 12.5 megohm resistors
   - Power per cell: 8.4 μW enabled, 6.8 μW disabled

3. Three Diodes (will work with higher pinchoff voltages while maintaining low power, but larger cell size)

   - 17 and 50 megohm resistors
   - Power per cell: 2.6 μW enabled, 2.0 μW disabled

4.2 Process Development

Seven wafer lots of RM2 wafers were completed during this time without encountering any particular processing difficulties. Once an acceptable fabrication technique for cermet resistors was found, it was incorporated into the standard processing line with minimal difficulty. The wafer yield (processing) for the seven RM2 lots was determined to be 81% and was limited primarily by wafer breakage and nitride lifting.

4.2.1 Parametric Data and Process Monitoring

Of particular importance to the RAM development are certain process monitor parameters which are indicative of how well the process is proceeding at the various stages of fabrication. Table 4.2-1 summarizes device parameters obtained for each RAM lot using processing routines successfully adapted for the RAM fabrication. The threshold voltages of FETs are all within an acceptable range, indicative of good process control. A more detailed des-

cription of the pinchoff voltage status will be discussed in a later paragraph. In the case of the logic diodes, the series resistance, R_s, and the threshold voltage, V_{TH}, have been monitored and again show acceptable values for all wafer lots. Finally, the ohmic contact measurements show that specific contact resistance, r_c, and the sheet resistivity, R_s, are all generally within normal values.

Table 4.2-1
Process Monitor Parameters for RM2 Wafer Lots
Numbers Shown are Average Value Per Lot

Wafer	FETs		Diodes		Ohmic Contacts	
Lot	V_p (V)	I_{DSS} (mA)	R_S(Ω)	V_{TH} (V)	r_c (Ω-cm^2)	R_S (Ω/□)
1	0.496	0.83	630	0.877	2.8×10^{-6}	417
2	0.518	1.12	627	0.818	3.2×10^{-6}	408
3	0.416	0.86	618	0.874	1.3×10^{-5}	315
4	0.510	1.18	632	0.859	2.3×10^{-6}	349
5	0.582	1.27	420	0.822	1.5×10^{-5}	333
6	0.660	1.30	694	0.940	4.5×10^{-5}	297
7	0.78	1.94	2474	1.09	4.1×10^{-6}	1152

4.2.2 Cermet Resistor Fabrication

The technique for megohm resistor fabrication begun during the AP1 mask phase continued to be developed for the RM2 arrays. The finished on-chip resistors, however, showed a considerable variation in resistivity value, and were not in good agreement with the four point probe measurements. After several attempts to fabricate resistors with consistent resistivity values, an Auger analysis of the cermet films was pursued in an effort to uncover problem areas, particuarly with espect to the cermet-to-second metal contact. Figure 4.2-1 shows the atomic fraction of the surface as a function of depth for a

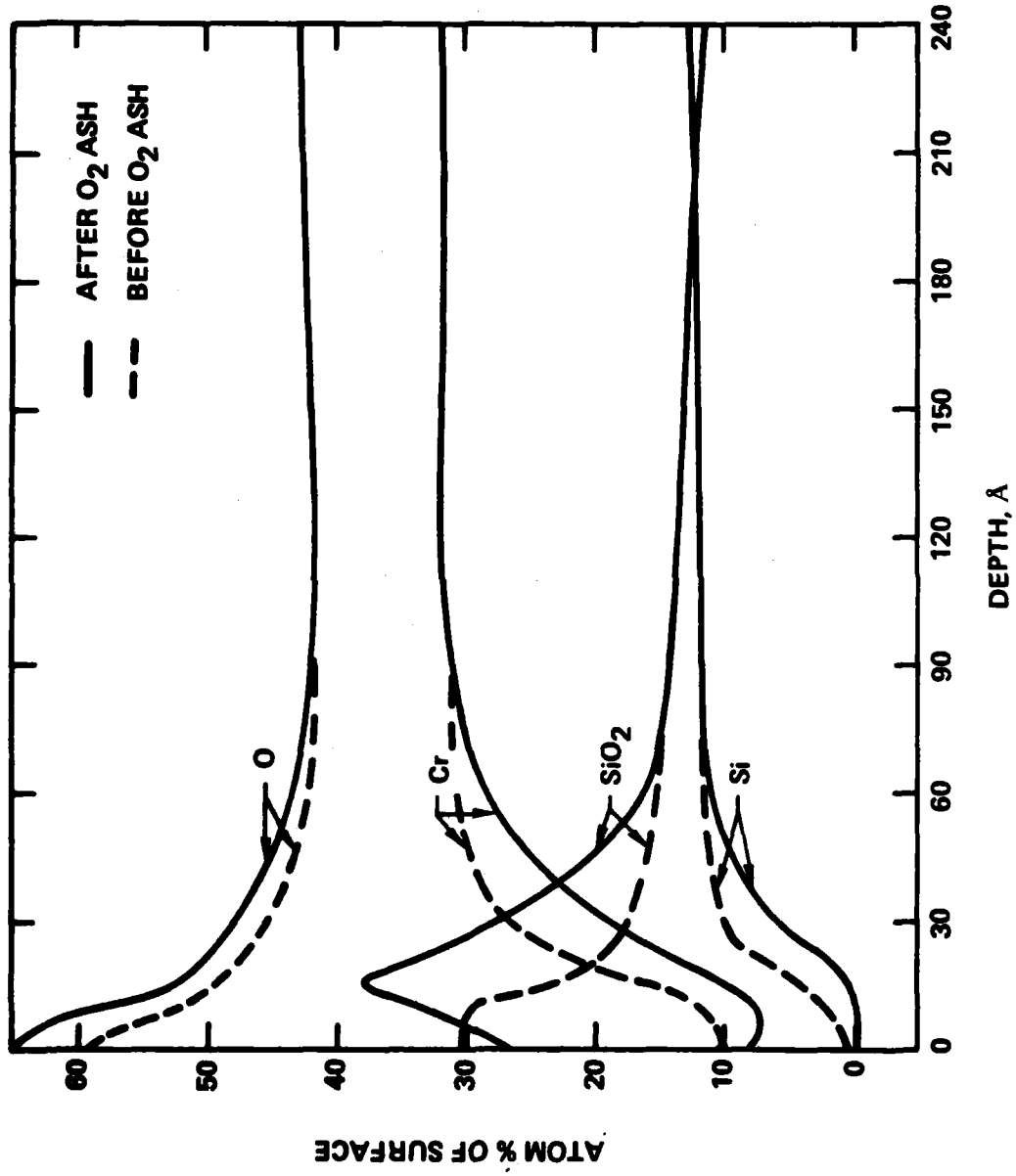

Fig. 4.2-1 Auger analysis of cermet film.

cermet film. The high percentage of oxygen and dielectric at the surface suggests the formation of an oxide layer after exposure of the film to air. The effect of O_2 ashing for photoresist removal can also be seen in the figure. This oxide layer would make the contacting to second-level metal very difficult, and could account for the spurious results which were initially observed.

One technique to avoid this problem was to simply interchange the cermet and second-level metal process steps. Instead of metal being deposited on the cermet film as originally proposed, cermet would be deposited on second-level metal (gold). This process is shown schematically in Fig. 4.2-2. Thus, the formation of oxides on the cermet film can be avoided, and since gold is relatively free of oxide, better contacts should result. Two test wafers (AP1-31 and AP1-32) were processed in which the cermet film was deposited on both wafers at the same time. However, wafer AP1-31 had second-level metal deposited on cermet, while wafer AP1-32 had the reverse process. Measurements of sheet resistivity for the two wafers are shown in Table 4.2-2. As can be seen, wafer 32 showed consistent results from the various techniques for measuring sheet resistivity, namely, a Van der Pauw "cross" pattern, a 22MΩ resistor, the transmission line method, and the mechanical four point probe.

Table 4.2-2

Resistor Measurements for Wafers AP1-31 and AP1-32

Wafer	Van der Pauw (MΩ/□)	22 Resistor (MΩ/□)	TLM (MΩ/□)	2 R_c (MΩ)	4 Pt. Probe (MΩ/□)
31	--	8	--	--	2-3
32	3.3	3.0	3.4	3.2	2-3

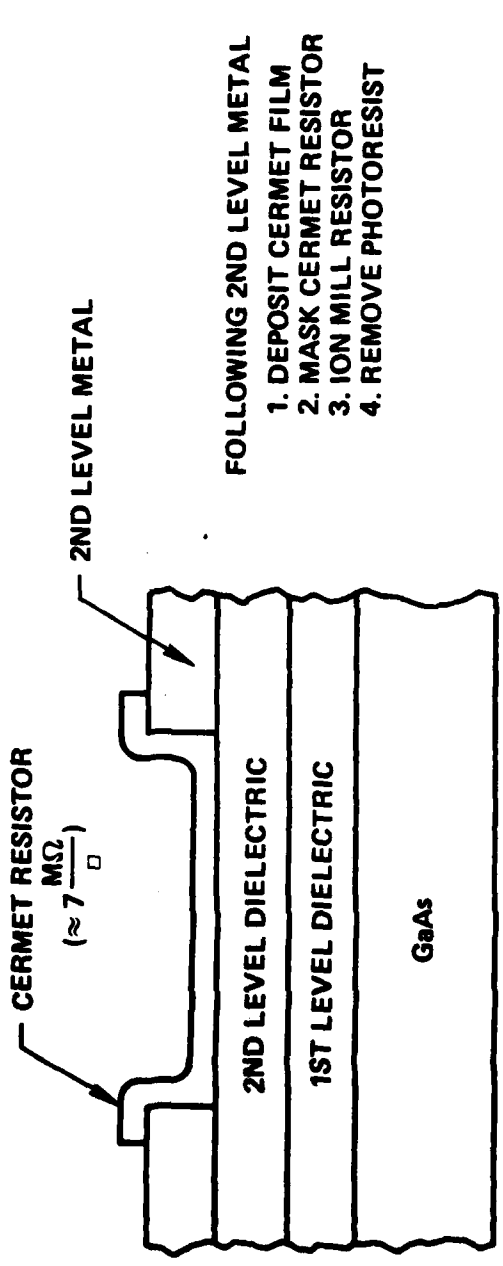

Fig. 4.2-2 Cermet resistor fabrication steps.

Measurement of wafer 31, on the other hand, showed inconclusive results and the inability to make most of the measurements due to open test structures or scattered data. The test showed, however, that deposition of the cermet film on second-level metal was the preferred process and, as a result, would be the technique used for the RM2 mask set.

One potential problem area with the above described approach is the step coverage of the thin (≈ 3000A) cermet film over the thicker (4000-6000A) gold interconnect layer. Figure 4.2-3 shows a SEM photo of cermet resistor over a second-level metal where the film thicknesses are 3000A and 6000A, respectively. The step coverage is reasonably good in this case, primarily due to the slight sloping of the ion milled metal line edges. In fact, the degree of slope of the metal edge can be controlled by the ion milling techniques use, and thus, offers some additional control if necessary.

The sheet resistivity value for the resistors fabricated with the RM2 (256 bit) mask set was chosen as a function of final resistor size and ease in which reproducible films could be deposited and, thus, dictated resistor sizes of 2 x 12 μm (6□) and 2 x 5 μm (2.5□). Processing of the resistors for all the RM2 wafers was done in a manner identical to that of wafer AP1-32 in which the cermet film was deposited on second-level metal. The RM2 mask set has test patterns for measuring sheet resistivity, resistor uniformity and contact resistance. Figure 4.2-4 shows one of these test patterns, as well as the completed resistors in a typical 256 bit RAM cell array. Table 4.2-3 shows the test data obtained for the seven RM2 wafer lots which were processed. The resistor values on the wafers were purposely kept below the design values of 50 MΩ and 22 MΩ so that ion mill thinning could be used later to optimize the resistor values. The uniformity of the resistor values over the wafer is also shown in Table 4.2-3. The measurements indicate that reasonably good results can be obtained using these fabrication techniques, and extension to a 4K RAM design should present no major fabrication difficulties.

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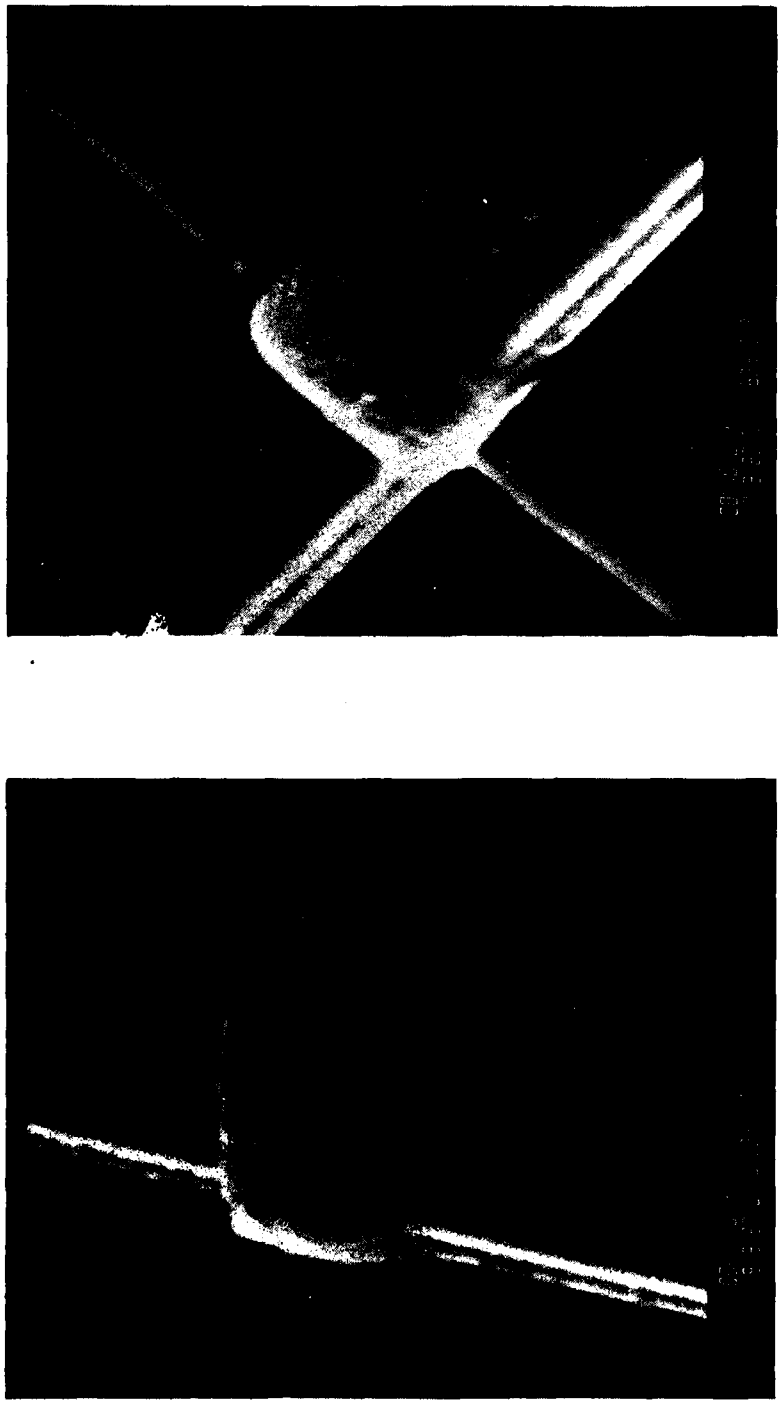

Fig. 4.2-3 Step coverage of cermet on second-level metal.

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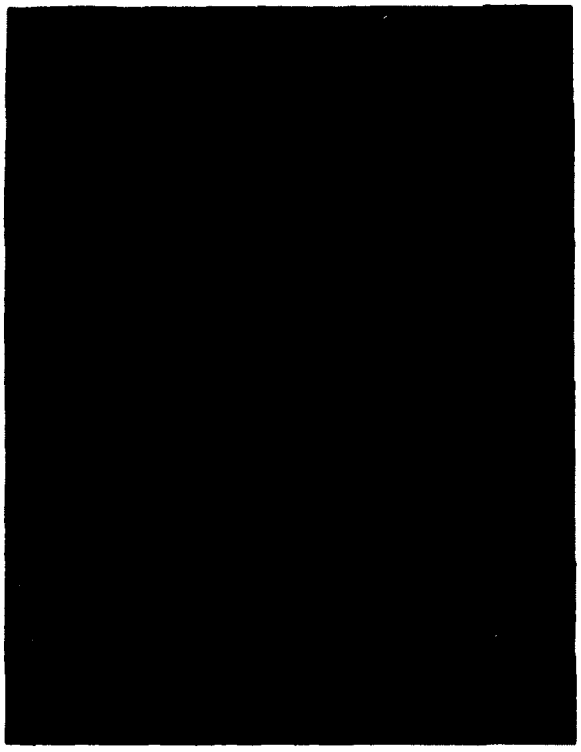
TEST STRUCTURE FOR SHEET RESISTIVITY AND CONTACT RESISTANCE



RAM CELL ARRAY SHOWING THE MΩ RESISTORS

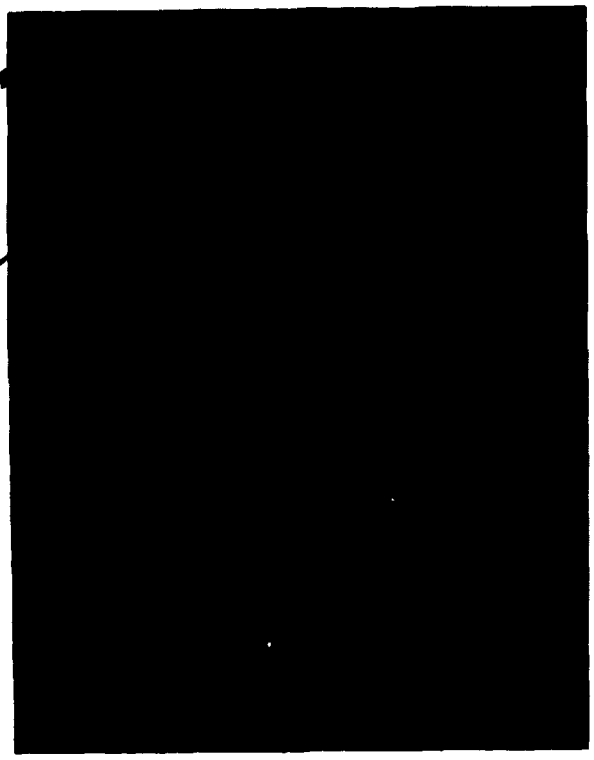


Fig. 4.2-4 Test structure and cell array for cermet resistors.

CONTROL OF CERMET RESISTOR VALUES FOR RM2 WAFERS

WAFER	SHEET RESISTIVITY (MΩ/□)	RESISTOR VALUES 6□ (2 x 12 μm) (MΩ)	RESISTOR VALUES 2.5□ (2 x 5 μm) (MΩ)	CONTACT RESISTANCE $2R_c$ (MΩ)
11	5.5	39.9 ± 7.8%	18.9 ± 7.8%	4.2
12	6.5	44.7 ± 6.2%	20.6 ± 7.8%	3.9
14	5.7	41.3 ± 8.6%	19.6 ± 8.1%	4.7
21	6.4	38.9 ± 7.0%	17.7 ± 6.9%	3.1
22	5.7	35.3 ± 3.7%	16.3 ± 3.2%	2.4
23	6.5	39.0 ± 4.0%	17.7 ± 6.4%	2.7
24	7.3	44.2 ± 14.5%	20.5 ± 14.4%	4.1
31	6.9	43.5 ± 7.9%	20.0 ± 8.2%	3.3
32	7.5	46.2 ± 5.8%	21.8 ± 6.9%	4.1
33	7.1	47.7 ± 7.0%	22.1 ± 7.5%	3.3
34	7.3	50.3 ± 7.8%	23.6 ± 8.5%	4.3
43	5.0	32.3 ± 6.3%	15.1 ± 5.9%	3.3
44	5.0	33.6 ± 4.5%	15.8 ± 4.4%	2.8
54	8.5	59.6 ± 4.5%	28.6 ± 4.9%	6.5
61	7.5	56.7 ± 6.4%	28.4 ± 6.8%	8.7
62	7.2	52.2 ± 7.2%	25.8 ± 7.3%	8.5
63	8.0	58.0 ± 10.9%	30.5 ± 12.3%	10.0
64	7.5	56.6 ± 6.6%	27.3 ± 6.5%	7.5
72	7.4	50.6 ± 7.5%	24.2 ± 7.7%	5.8
73	8.0	59.9 ± 13%	29.6 ± 14.8%	9.8
74	7.3	56.6 ± 9.7%	27.7 ± 11.5%	7.4
AVERAGE	6.85	47 ± 7.5%	22.5 ± 8%	5.3

4.3 RM2 Test Results

The testing phase of RM2 wafers consisted of two parts. The first part was the yield testing of undecoded 224 bit arrays, while the second part demonstrated the functionality of decoded circuits. During the course of the testing program, substrate isolation was found to play a significant role in the operation of the arrays. As a result, more detailed measurements were made of leakage currents and correlations made to the operating characteristics of the cell.

4.3.1 Array Testing

Testing of the undecoded arrays on RM2 wafers was done using an automated probe station and an Analog Devices MACSYM test computer. The test program exercises each cell in the RAM, reads the output and compares it against threshold, and prints out errors. It also tests for storage of an initially written "1" after disabling and re-enabling.

The test program goes through the following steps: It applies power to the circuit for testing; prints out current values and aborts the test if it finds a short; then cycles each cell in turn five times, writing alternately "0" and "1" leaving cells in the "1" state as it disables each row. After this cycling, each cell is addresssed in turn. For each cell, 1) the output is read, digitized by comparing it to a reference and an error flag set true or false, 2) a "0" is written, digitized, checked for error, and 3) a "1" is stored in a matrix by row, column and test condition (1, 2 or 3 above), as well as an error map (0 for no error, 1 for error) with the same matrix coordinates. While the test is in progress, any errors caused a printout (on the CRT) of address, test condition failed and analog output voltage. At the conclusion of the test, a failure summary is printed out of the:

1. Number of cells failing to write a "0" or a "1",
2. Number of cells failing to write a "1",
3. Number of cells forgetting a "1" after being disabled,

4. Number of cells that failed both 2 and 3 above,
5. Total number of failures (both forgetting and failing to write).

The failure rate of the 224 arrays is shown in Table 4.3-1 where the test results can be divided into three yield classifications. The first category showed an acceptable yield and is represented by the first four wafers (11 through 21). The second category showed relatively low yield and is represented by wafers 22-24. The final set of wafers showed no yield and is represented by wafers 31-72. In an effort to determine the cause of the array failures, a number of electrical measurements were made. The substrate isolation characteristics were of primary importance and detailed measurements were made for each yield category. The standard isolation gap which was used in making the measurements is shown schematically in Fig. 4.3-1, along with the substrate I-V characteristics for each of the yield categories mentioned above. The curves generally have a threshold voltage in the range of 0.5 to 2.0 V and are consistent with the carrier-injection phenomenon based on the Lampert-Rose model.[5] The initial indication, therefore, was that the cell yield was directly related to the substrate isolation properties, but that more testing would be required before making any final judgements.

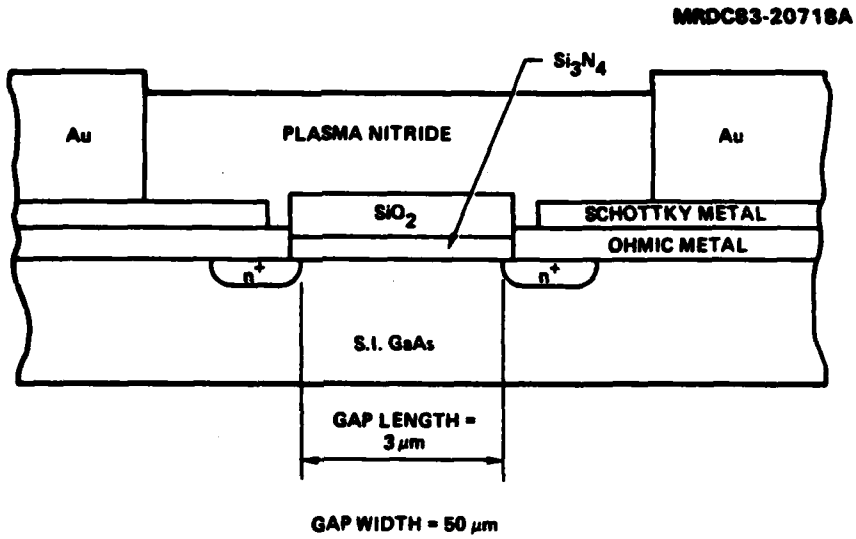
To further evaluate substrate leakage effects, a number of measurements were made on individual RAM cells. Since the proper voltages at the drain nodes of the three switching FETs are crucial to successful cell operation, a direct measurement of gate voltage vs the three node voltages was made. After grounding one of the nodes and applying voltage to the second node, the gate voltage at the third node was monitored. For a high yield wafer (Fig. 4.3-2), the gate voltage for the three FETs remains constant at ≈ 1.0 V as the drain voltage varies from 0 to 2.5 V. For low yield wafers,

Table 4.3-1

224 RAM Cell Arrays
Number of Failures (36 Arrays/Wafer)

Wafer Number	00	1	2	3-14	Partials < 100	> 100
11	3	2	3	8	18	2
12	3	7	5	9	12	-
14	5	3	5	11	8	4
21	3	3	2	-	26	2
22	-	-	-	3	22	11
23	-	-	-	1	8	27
24	-	1	1	9	17	8
31	-	-	-	-	2	
32	-	-	-	-	1	
33,34	-	-	-	-	-	
43,44	-	-	-	-	-	
54	-	-	-	-	-	
61,62,63,64	-	-	-	-	-	
72	-	-	-	-	-	
73	-	-	-	2	24	10
74	-	2	1	8	15	10

Figs. 4.3-3 and 4.3-4, the gate voltage does not remain constant with drain voltage, but rather decreases significantly, the 2 μm left FET being the most sensitive. These results suggest that a leakage path exists between the gate and drain of the FETs, and that measurement of specific FET characteristics would be needed to further isolate the problem. The subthreshold current characteristic of a single isolated FET is shown in Fig. 4.3-5. This measurement shows a perfect characteristic with negligible gate current in the range of V_g = 0 to -1.0 V. However, when measuring subthreshold characteristics of FETs within a RAM cell, even the high yield wafers showed signs of increasing



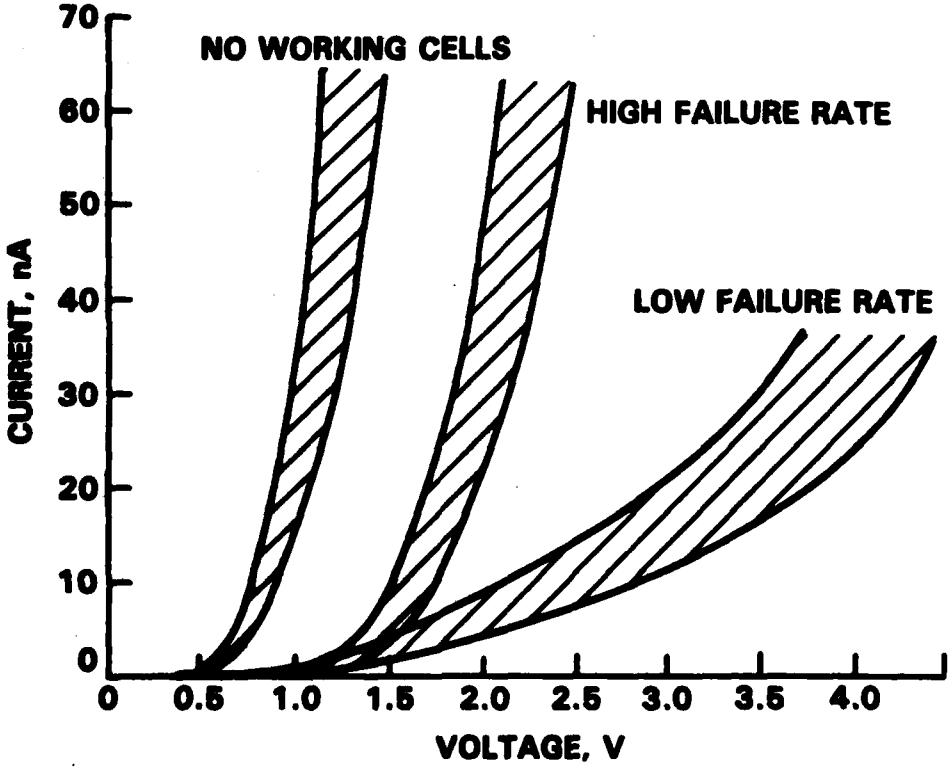


Fig. 4.3-1 Isolation characteristics of 50 x 3 μm isolation gap for the three categories of cell yield.

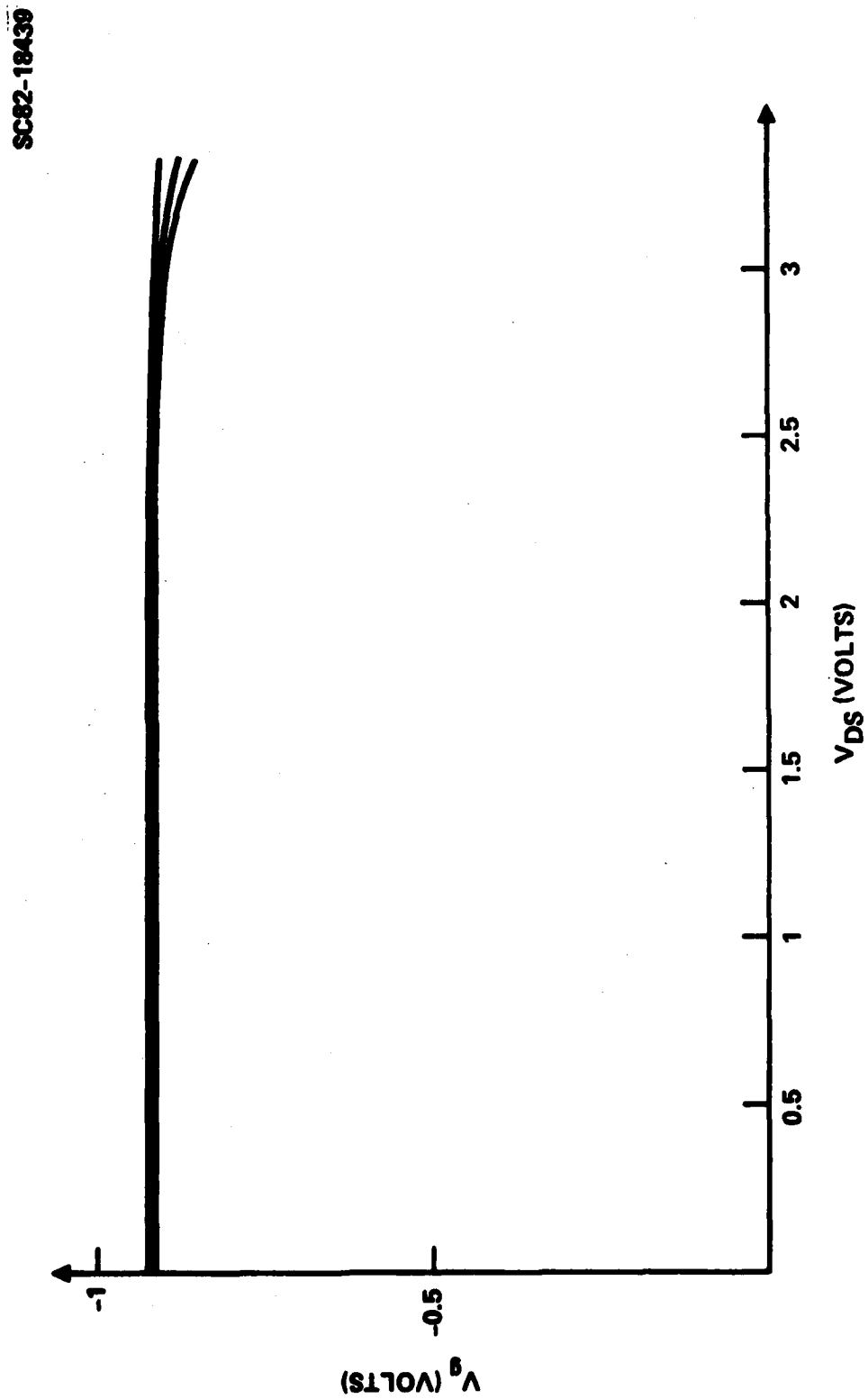


Fig. 4.3-2 Gate voltage characteristics for high yield wafer.

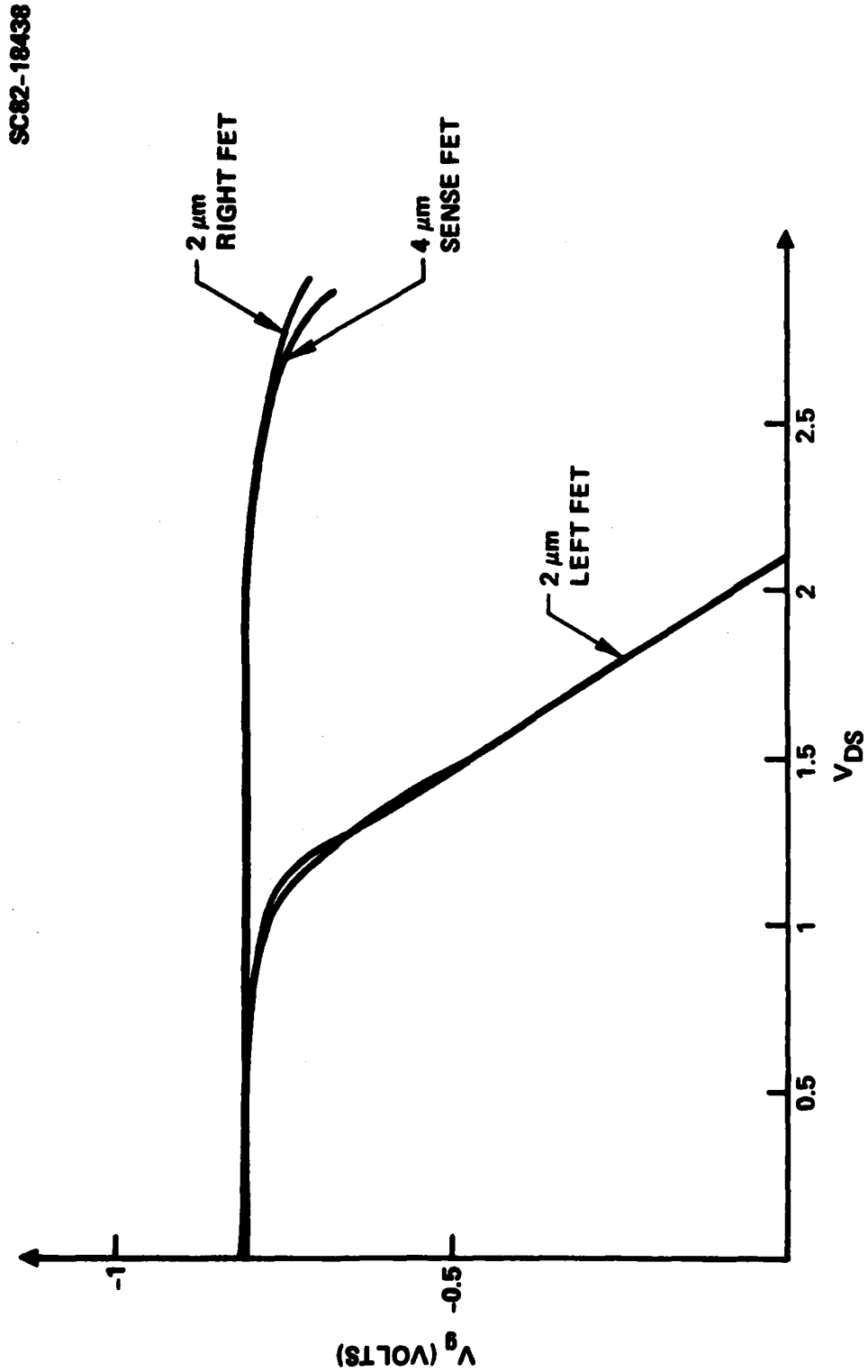


Fig. 4.3-3 Gate voltage characteristics for low yield wafer.

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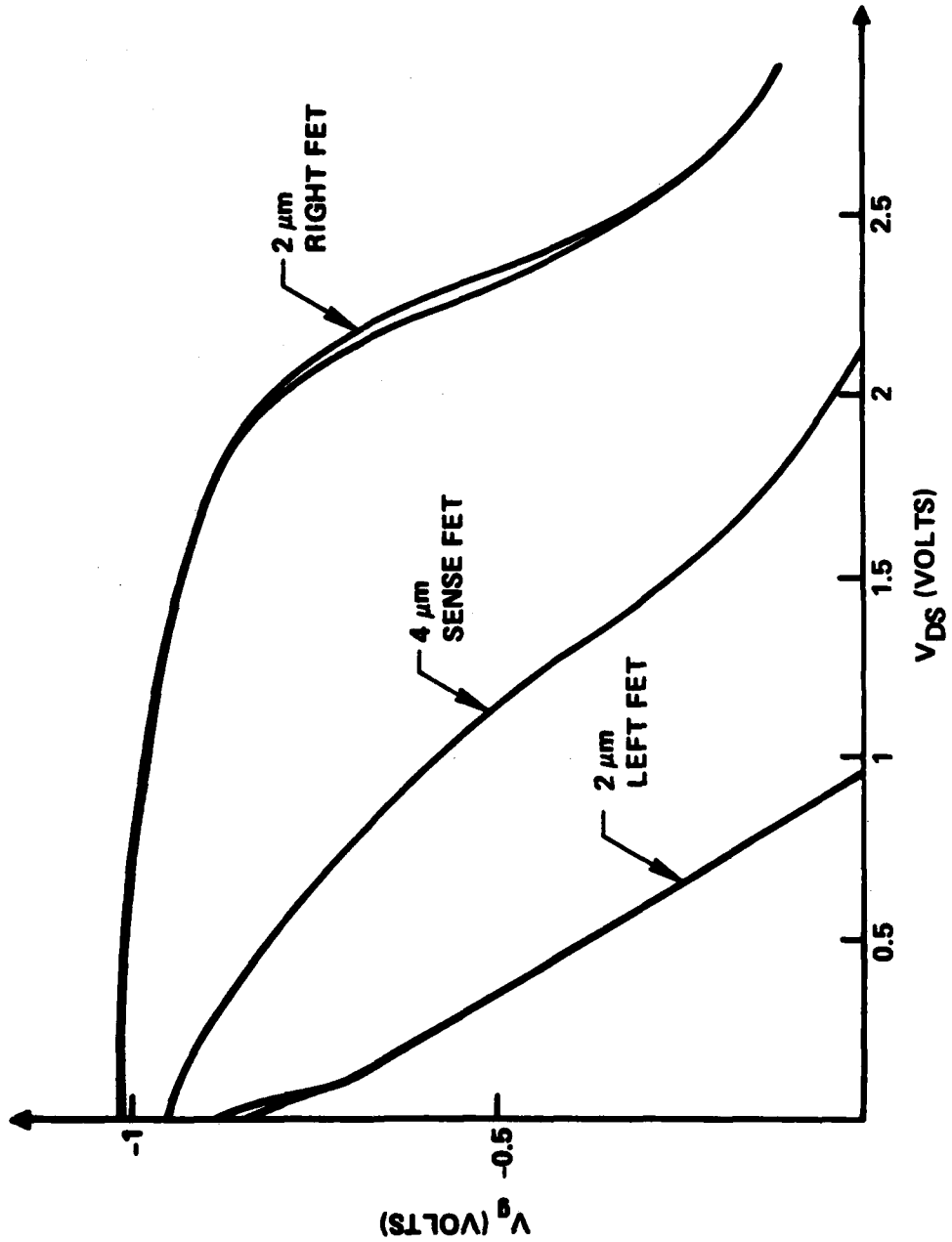


Fig. 4.3-4 Gate voltage characteristics for zero yield wafer.

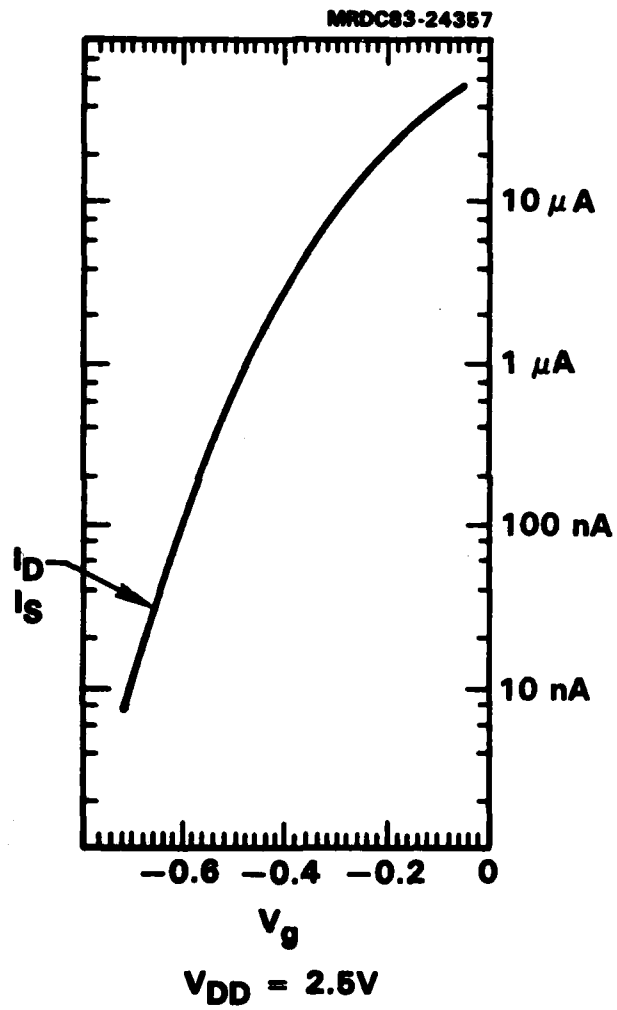


Fig. 4.3-5 Drain and source current characteristics for an isolated 4 μm FET.

gate current as shown in Fig. 4.3-6a. The results were even more dramatic for low and no yield wafers where the gate current is unusually high (Fig. 4.3-6b). This high current causes a high drain current when the gate voltage is negative, thus resulting in cell failure. Thus, the first order mechanism for low power RAM cell failure was, at this stage, substrate leakage which, in turn, degraded the subthreshold FET characteristics. One possible means for the improvement of substrate isolation is by ion bombardment. Proton implantation was investigated for this purpose and is discussed in detail in the following section.

4.3.2 Isolation Tests

Proton implantation in semi-insulating substrates has been used for several years as a means to increase device isolation and to reduce the backgating effect.[6] This improvement was initially attributed to the increase of resistivity caused by proton damage. More recent experiments,[7] however, have shown that backgating improvements were realized, not because of resistivity increases, but because of an increase in the threshold for substrate conduction. Thus, it appeared that proton isolation would be an effective means of improving interdevice isolation for RAM cells.

One of the first experiments to be performed before proton bombardment could be incorporated into the RAM process was to determine the necessary implant parameters for optimum isolation. Figure 4.3-7 shows the I-V characteristics of a standard 50 x 3 μm isolation gap with and without proton implant. The case shown is for 150 keV, however, energies as low as 100 keV were also found to be effective. Implant energies of 75 keV or less were not deep enough to provide consistent isolation properties. Proton doses in the range of 1-4 x 10^{14} H^+/cm^2 were found to be optimum, while higher doses led to a decrease in resistivity.

The improvement in device isolation by proton bombardment indicates that the current leakage path in the substrate is probably very close to the surface. One possible reason for such surface leakage is the outdiffusion of

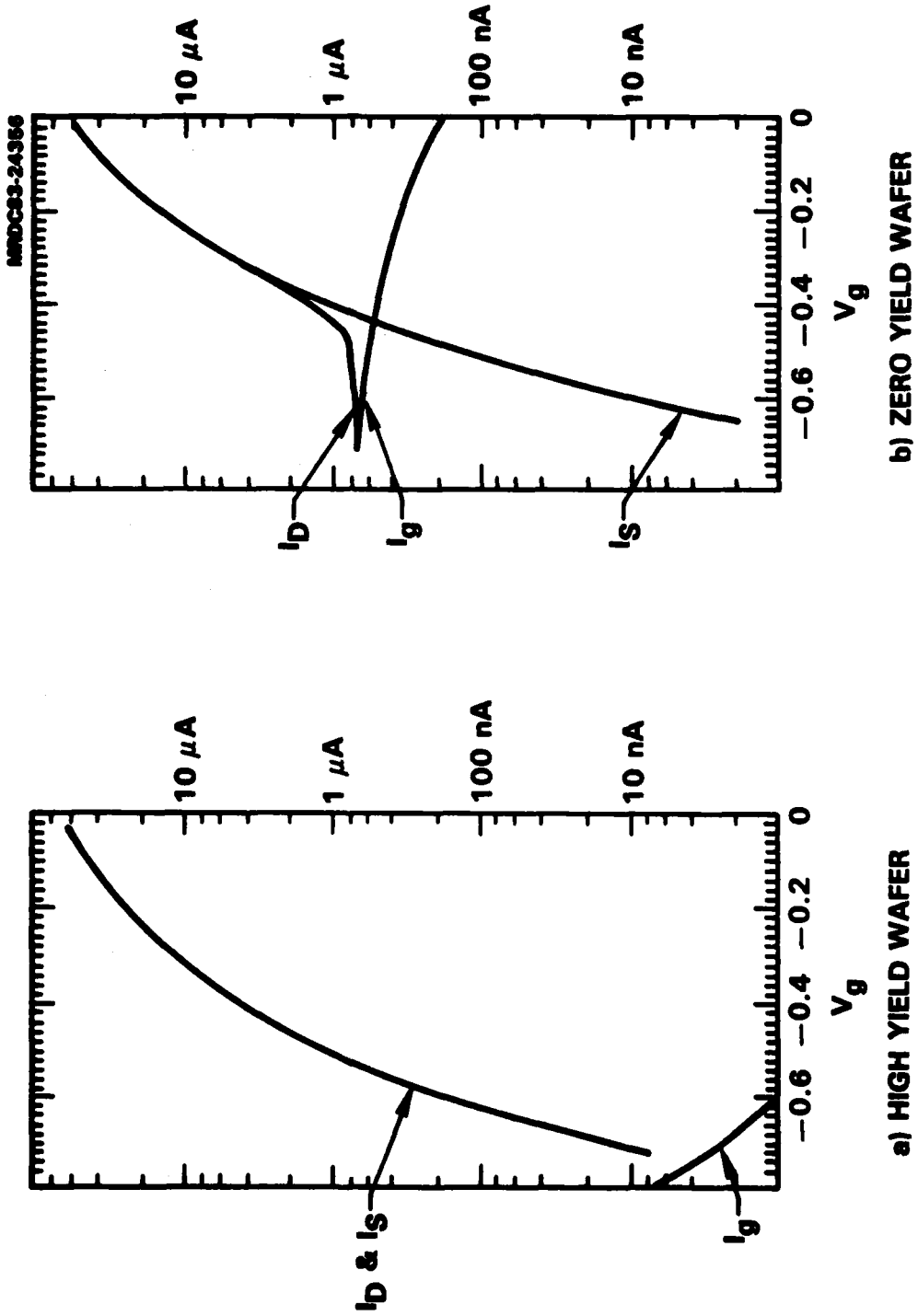


Fig. 4.3-6 Drain and source current characteristics for RAM cell FETs.

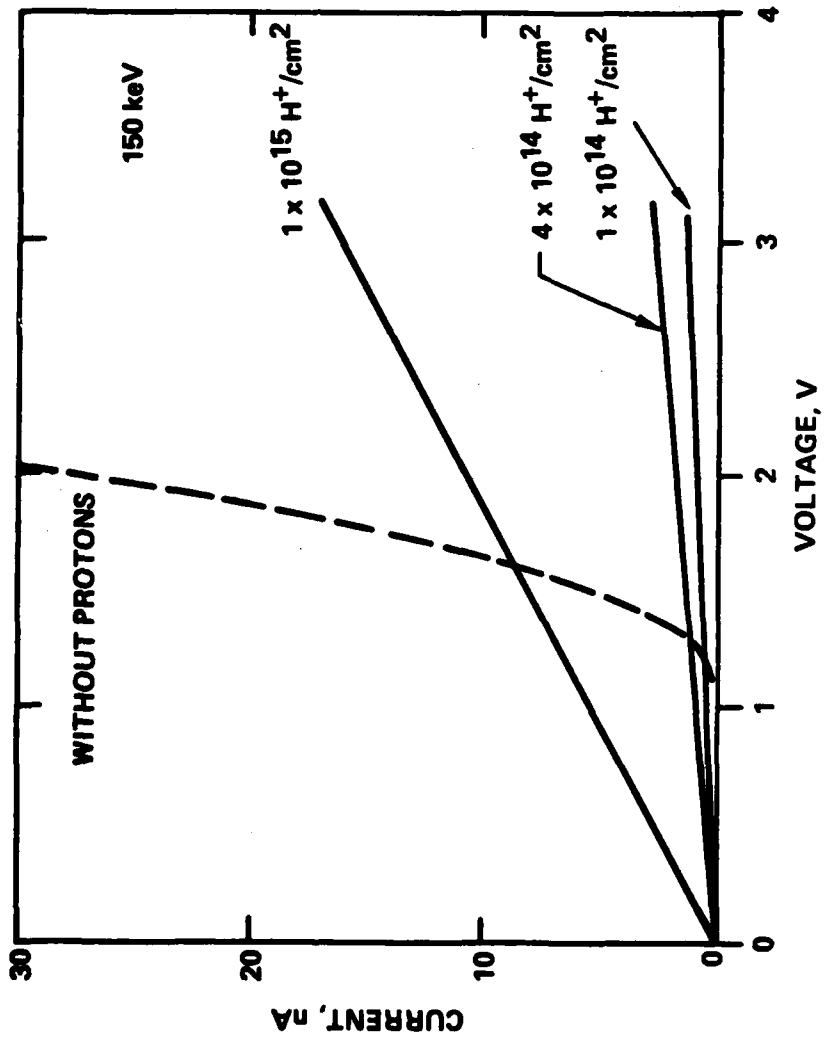


Fig. 4.3-7 Measurement of proton isolation characteristics using a 50 x 3 μm isolation gap.

EL2 during the post-implantation annealing.[8] Because of fewer traps at the surface, the trap-fill-limited voltage or the threshold voltage for current conduction near the surface is smaller than in the bulk, therefore, the surface leakage is higher. With proton bombardment, the number of traps is increased so the threshold for current leakage is also increased. Besides the trap-filling model, there is another possible explanation for the improvement made by proton isolation. Because of the proton damaged layer, the potential distribution in the substrate may be changed and some local high field regions may be eliminated. Thus, the instability associated with high fields and the resulting nonlinear substrate current conduction no longer exists.

The implementation of a proton bombardment step into the RAM process is shown schematically in Fig. 4.3-8. The step occurs after ohmic metal alloying and utilizes a 2.5 μm thick photoresist as an implant mask. The mask is somewhat larger than the actual size of the active area in order to allow for lateral spread of the protons. Once the proton implantation has occurred, the photoresist is stripped off and normal processing resumes.

The effectiveness of proton isolation was demonstrated on a RAM test wafer, RM2-81. One half of the wafer was fabricated in the standard fashion, while the other half was processed with a proton isolation step. Testing of the 224 bit undecoded arrays showed a significant decrease in the failure rate for the proton implanted side. Not only was the failure rate reduced from 12% to 2.5%, but the proton implanted side had three perfect arrays while the non-implanted side had none. Thus, the effectiveness of proton bombardment as a means of reducing substrate leakage was demonstrated, and henceforth would become a necessary procedure for the fabrication of the ultra-low current devices.

On additional test which was performed on proton isolated samples addressed the issue of proton damage reliability. Since the highest temperature the wafers experience following proton implantation is 250°C, a test sample was baked at this temperature for 40 hours. No degradation of isolation was noted following this test. The temperature was then raised to 275°C

MRDC83-24333

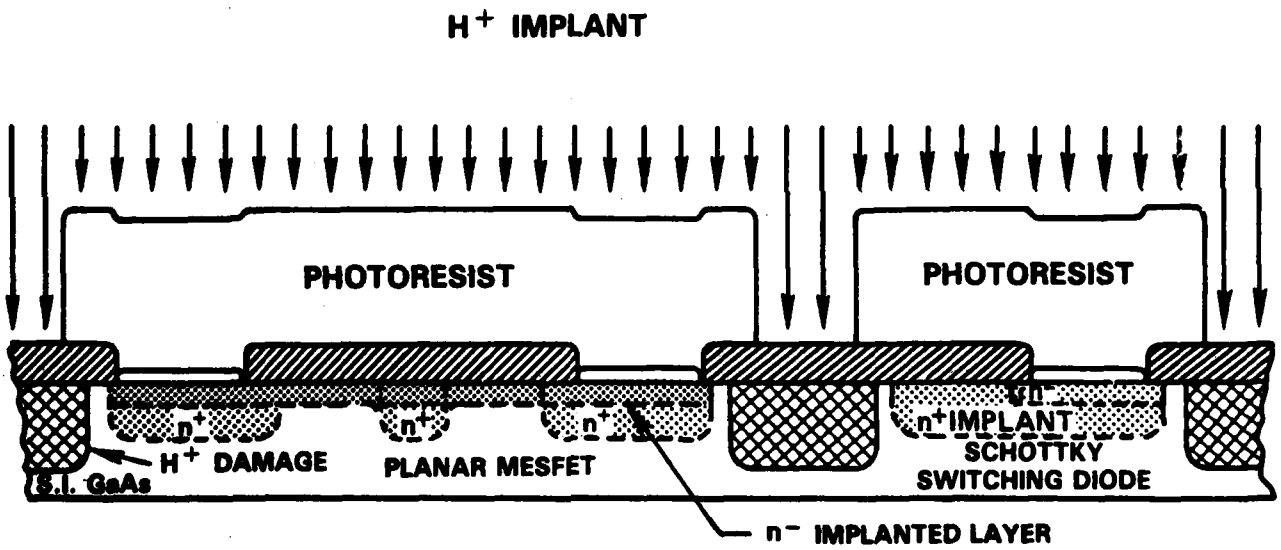


Fig. 4.3-8 Schematic cross section of the proton isolation step.

for a period of 65 hours, and then finally raised to 300°C for 92 hours. Again, no change in the leakage characteristics was noted during this time. This result is consistent with other reported results,[6] and indicates that proton isolation should be an acceptable technique for incorporation into RAM array processing.

5.0 RM3 MASK SET

The demonstration of a fully functional 256 bit static RAM was based on knowledge gained with the two preceding mask sets. A number of design and processing modifications were incorporated with mask set RM3, the most important being the implementation of a 3 inch wafer process. The design and layout considerations are discussed in Sec. 5.1, while wafer processing is described in Sec. 5.2. The testing of RAM wafers is discussed in Sec. 5.3 along with preliminary yield considerations.

5.1 Mask Set RM3 Design and Layout

The main objective for designing mask set RM3 was to launch the processing of 3 in. diameter GaAs wafers. The 256-bit RAMs on mask set RM3 are very similar to those on mask set RM2, except for relatively small corrections and design improvements. The main changes from mask set RM2 to mask set RM3 were related to die organization and alignment marks for processing with a 10 X wafer stepper on 3-inch wafers. Mask set RM2 contained a number of different versions of the 256-bit RAM, some with and some without peripheral circuits. Several versions were also included in RM3, but the number of different options was smaller. RM3 provided an opportunity to add a number of test structures consisting of portions of the peripheral circuits and single cells which were extracted from the full RAM circuits. This addition was very important because mask set RM2 lacked these diagnostic elements. A photograph of mask set RM3 is shown in Fig. 5.1-1.

On mask set RM3, the design of the RAM cell was still at a more advanced stage than the design of the peripheral circuits. The design of the RAM cell had already undergone one iteration following extensive characterization. The peripheral circuits instead, were the result of a first simple design to provide a vehicle to address the memory array without any attempt to attain low power dissipation. Fine tuning of the peripheral circuits so that their power dissipation is commensurate with the power dissipation of the memory cell array was left for a future design iteration.

MRDC83-24565

MASK SET RM3
256 BIT LOW-POWER GaAs STATIC RAM

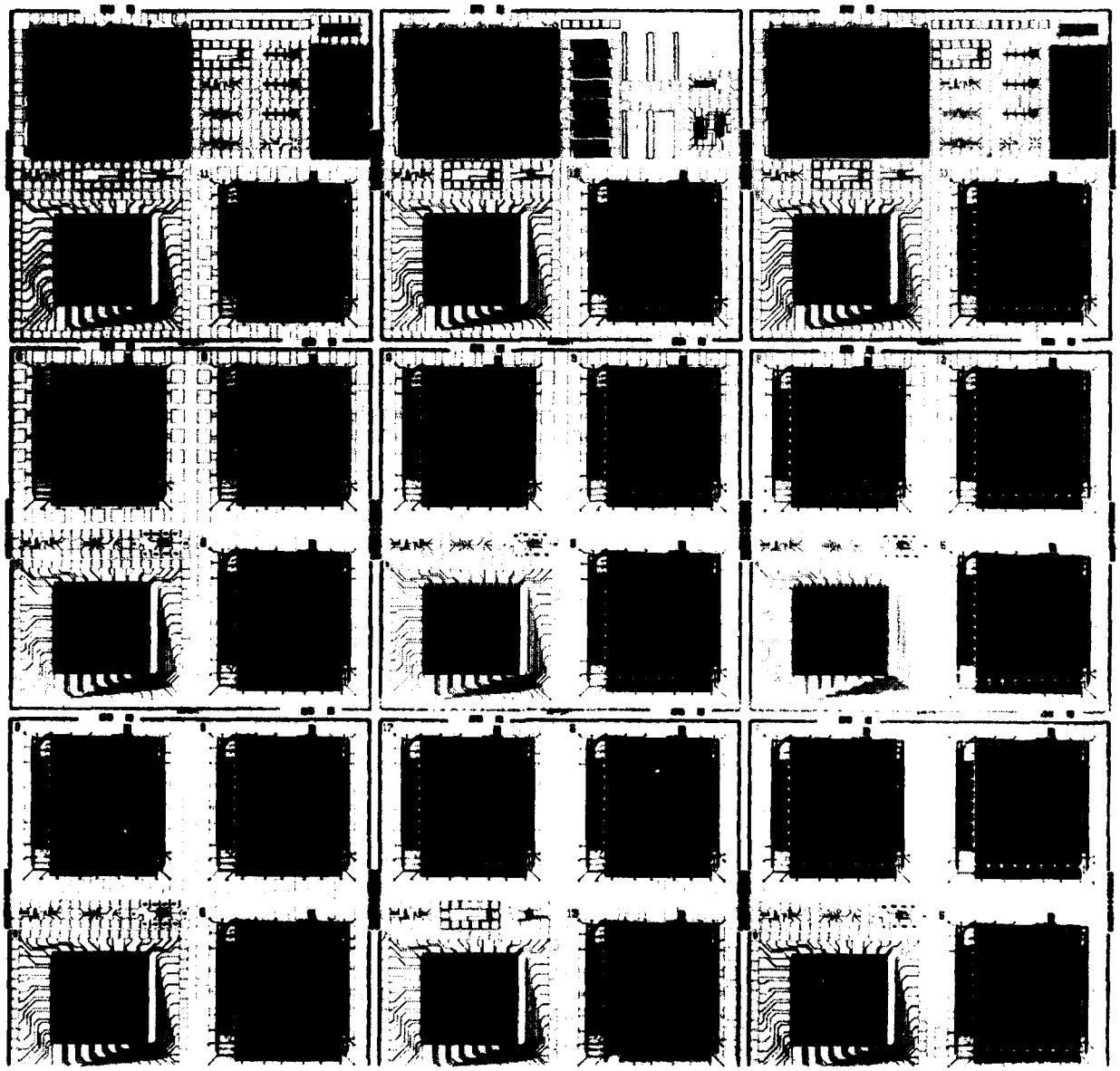


Fig. 5.1-1 Photograph of mask set RM3 containing several 256 bit static RAMS, some 224 RAM cell arrays (undecoded) and test structures. This mask set was used to process 3 in. wafers.

5.1.1 256-Bit RAM Cell Design

A schematic of the typical RAM cell used on a mask set RM3 is shown on Fig. 5.1-2. This cell is virtually unchanged with respect to the cell used on wafer RM2, and it is designed to dissipate 1.6 μW. The only appreciable change was on the width of the transistor which drives the bit sense line. This width was increased from 4 to 7.5 μm. However, the version of the RAM cell with the 4 μm wide driver transistor was also retained. A higher-power low-resistor value version of the RAM cell which had been used on mask set RM2 was dropped from set RM3. A version having three level shifting diodes, supposedly capable of higher tolerance to FET threshold shift, was left on mask set RM3, although preliminary test on mask set RM2 indicated that it was not a worthwhile option. The layout of the cell was also left unchanged except for minor corrections on line spacings. The cell dimensions were 51 × 39 μm.

5.1.2 Peripheral Circuit

A schematic of the peripheral circuits used with the 256-bit RAM is shown on Fig. 5.1-3. This is a fairly conventional circuit. As on mask set RM2 the row and column address decoders require both the address and its complement. The complements could have been generated on chip by inverters, but then line drivers should have been provided. To keep the design as simple as possible, both the address and its complement were required from the inputs.

The column decoder circuit uses a NOR gate and a source follower driver. Source follower drivers were widely used in the peripheral circuits and are shown on Fig. 5.1-3. Although source followers have excellent drive capability, they consume too much power because their transistor is always on. In order to experiment with a power saving alternative the row decoder (which was identical to the column decoder on mask set RM2) was redesigned on mask set RM3. As shown on Fig. 5.1-3, the row decoder senses the address through a NAND operation performed by an SD^2FL gate having a complementary driver. Although a final chip design will have only one type of decoder, the two different designs used for rows and columns provided an opportunity for an

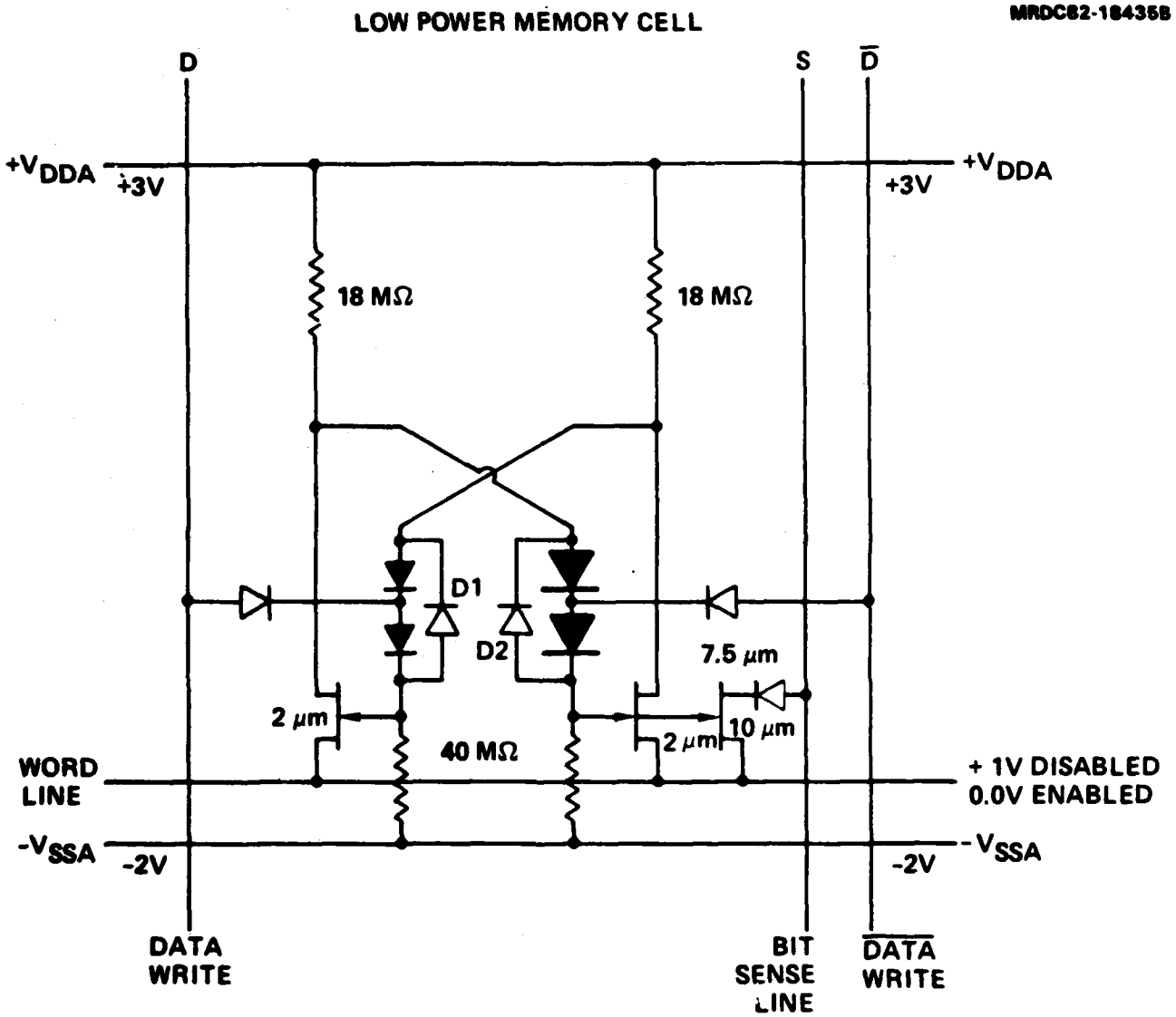


Fig. 5.1-2 Schematic of a typical cell used in the 256 bit GaAs static RAM on mask set RM3.

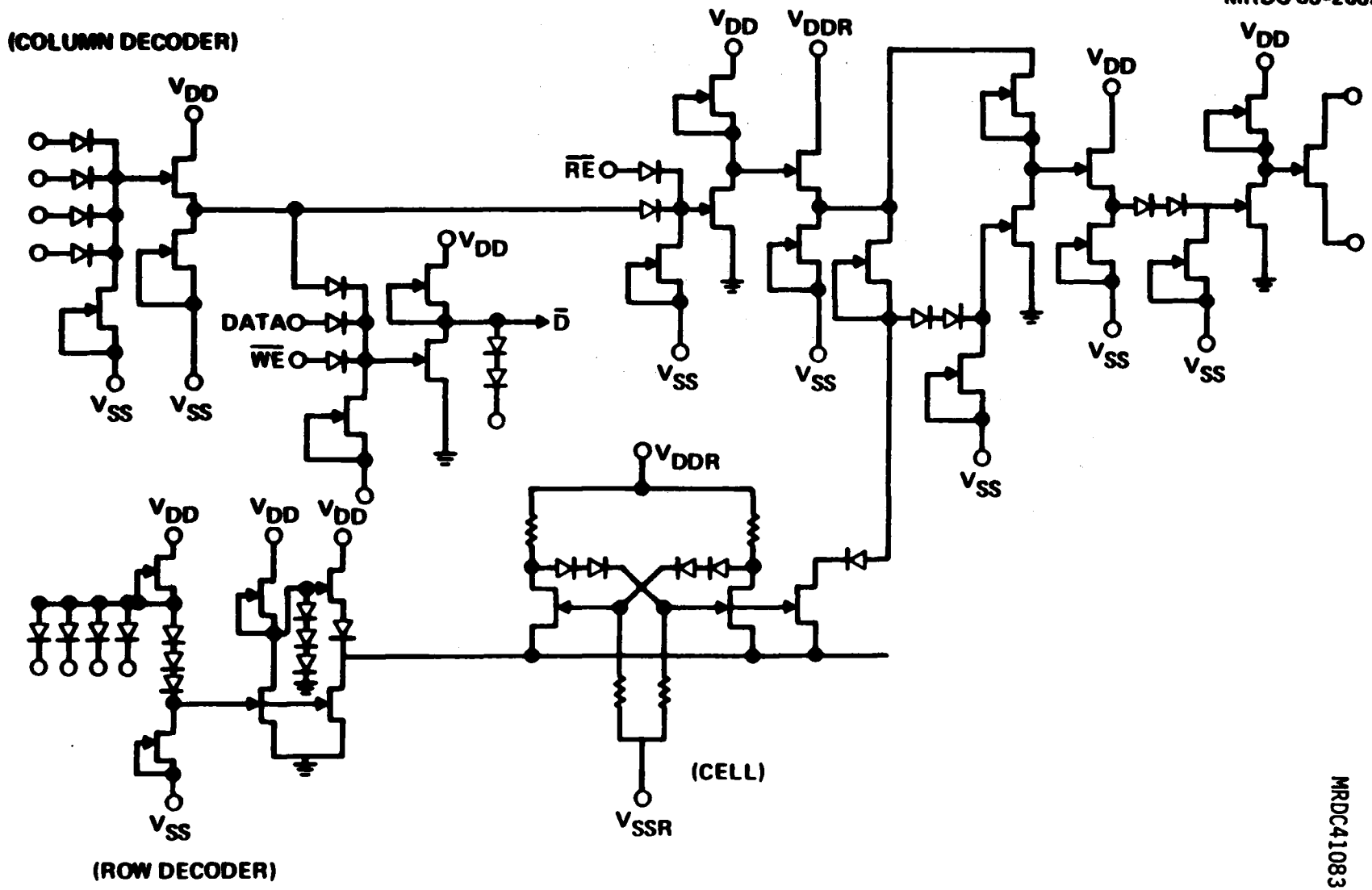


Fig. 5.1-3 Schematic of the peripheral circuits of the 256 bit RAM on mask set RM3.

experimental comparison of the trade-offs between the source follower and the complementary driver options.

5.1.3 Test Structures

A deficiency of mask set RM2 was lack of the test structures for the peripheral circuits. This was remedied on mask set RM3 by extracting every component of the peripheral circuits, placing it in a test cell, and connecting every significant electrical node to a row pad. Although not useful for high speed testing, these test structures provide an excellent tool for analyzing the operation of the circuits, particularly with respect to voltage levels and voltage swings. Since RM3 was the first mask set for processing of 3 inch wafers, some process yield related test structures were also incorporated. These test structures, which appear on the top row on Fig. 5.1-1, consist of long meander lines of first and second layer metal to test for shorts between parallel lines and between crossovers. A test structure consisting of long first to second layer interconnects was also incorporated on the mask set. A fairly dense array of standard test structures for characterizing the uniformity of device and ohmic contact characteristics was also incorporated. These process related test structures with a spacing of 2.8 mm in both directions, provide 396 data points on a 3 inch wafer.

5.2 Three-Inch Wafer Processing

The following section outlines the primary features of the transition from 1 inch to 3 inch wafers. In addition to an extensive equipment modification program, the techniques for handling and processing 3 inch wafers were undertaken with the ultimate goal of achieving process control and wafer uniformity. The details of the cermet resistor process and the new proton isolation step were finalized during this time and incorporated into the new processing line.

5.2.1 Equipment Upgrading for 3-Inch Processing

Prior to the fabrication of the first RM3 wafers, the entire process line was changed from 1 inch square wafer format to 3 inch round wafers. During this time, every piece of processing equipment was either modified to accommodate the larger substrate size or replaced by new equipment. The major investment was in the lithography area with the acquisition of a Censor 10X wafer stepper. This machine is capable of 1.0 μm dimensions with overlay accuracies of better than 0.25 μm (mean + 3σ). The field size was set at 8.4 x 8.4 mm, thus enabling the exposure of 44 full fields per wafer. All areas of dry etching were upgraded for 3 inch wafers and a new reactive ion etcher was brought on-line. Several new etching gases were used in this system to determine the best selectivity of SiO_2 to photoresist. All metalization systems utilized planetary substrate holders for uniformity control, and were equipped with instrumentation for deposition rate and film thickness monitoring. The cermet deposition system was changed from 6 inch diode sputtering to 8 inch magnetron sputtering. Again, planetary fixtures were used for film uniformity.

5.2.2 RAM Process Status

The intent of the initial 3 inch wafer processing was to use the RM3 mask set as the vehicle for establishing a 3 inch wafer line and, at the same time, trying to achieve operational 256 bit RAM arrays. This approach was a formidable one, since processing experience had to be gained while simultaneously fabricating a complex circuit design. As a result, the first two wafer lots were devoted to the process implementation through the Schottky metal level. The following two lots were used to finalize the proton bombardment steps, establish second-level processes, and fabricate cermet resistors. Finally, with the fifth and sixth lots, the entire process was proven feasible with 3 inch wafers and thus established a baseline for all future processing.

One of the primary concerns of the 3 inch process for RAM circuits was the control of the threshold voltage. A history of average pinchoff voltage for the initial wafer lost is shown in Fig. 5.2-1. The average value was fairly well-controlled to within the allowable limits for RAM fabrication, however, the standard deviation per wafer for these initial lots was not as good. As shown in Fig. 5.2-2, the deviation was generally greater than 100 mV and is probably due to the nonuniformities of certain pieces of process, such as the CVD oxide system and the reactive ion etcher. A more thorough investigation of uniformity will need to be made as soon as more data from 3 inch wafers in available and more consistent trends are noted. The fact that the processing rather than the material itself leads to nonuniformity in pinchoff is shown in Fig. 5.2-3. The depletion voltage, as measured by C-V profiles, is compared to the FET data. The results are generally in favor of the material, indicating more processing work rather than material selection will be required for better uniformity control.

The other aspect of 3 inch wafer processing which is unique to RAM arrays is the cermet resistor process. As mentioned previously, a new magnetron sputtering system with planetary wafer fixturing was employed for this step. Because this was a fairly significant change in processing equipment, a number of calibration runs and film measurements needed to be made. The basic process of cermet deposition on top of second-level metal remained unchanged, as did the resistor definition by ion milling. However, with the new magnetron sputtering system, the film resistivity was found to be very sensitive to the argon sputtering pressure. This relationship is shown in Fig. 5.2-4. The effects of post-deposition annealing at 200°C is also shown in the figure. Although the curve is very steep, fairly repeatable results could be obtained by careful regulation of the argon flow rate. The temperature coefficient of resistance (TCR) for these cermet films was also of interest, and preliminary measurements were made in the temperature range of 0-50°C. As shown in Fig. 5.2-5 the TCR for these films is always negative and decreases in magnitude as the resistivity decreases. These values are in reasonable agreement with

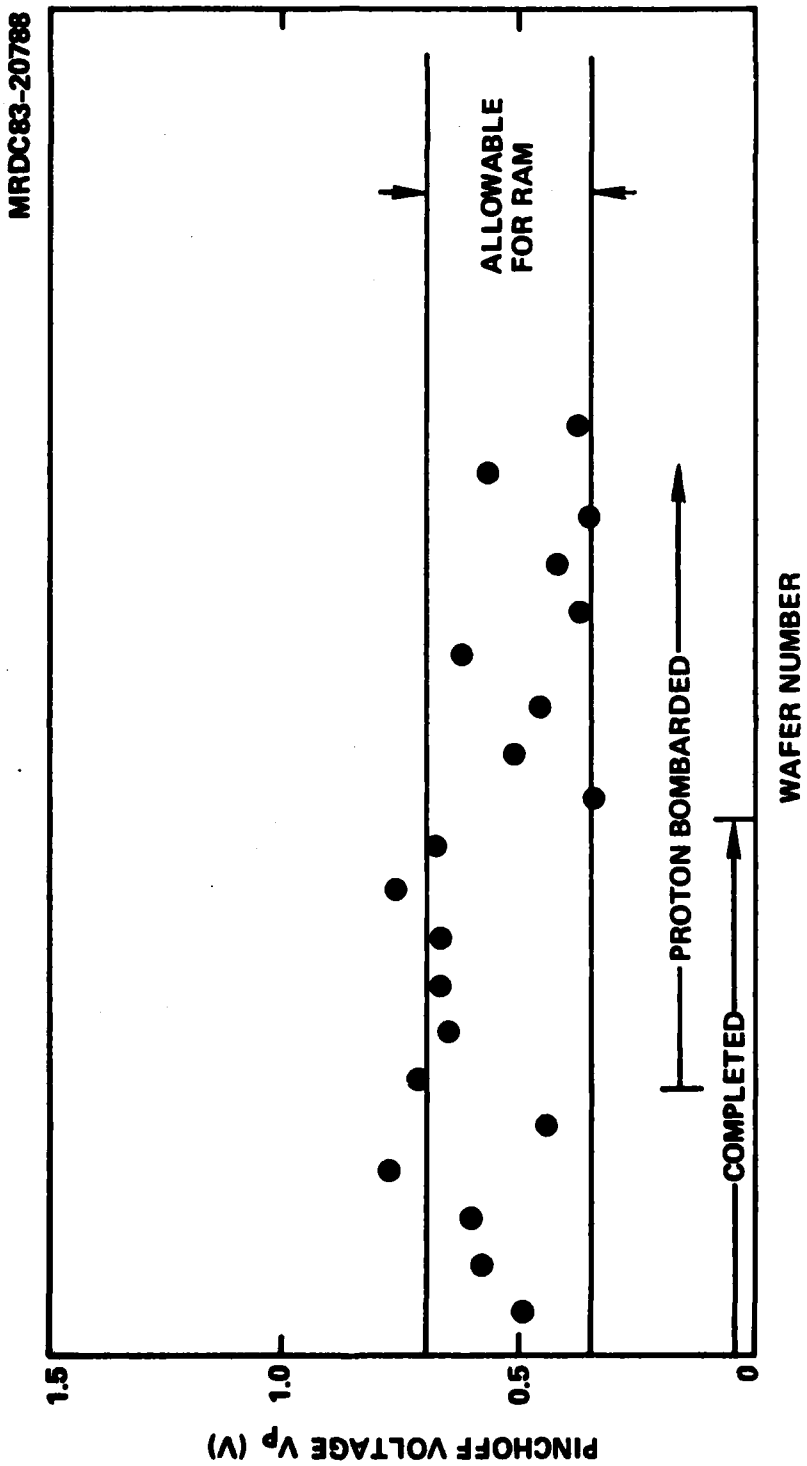


Fig. 5.2-1 FET pinchoff voltage (wafer average) for initial 3 in. RAM wafers.

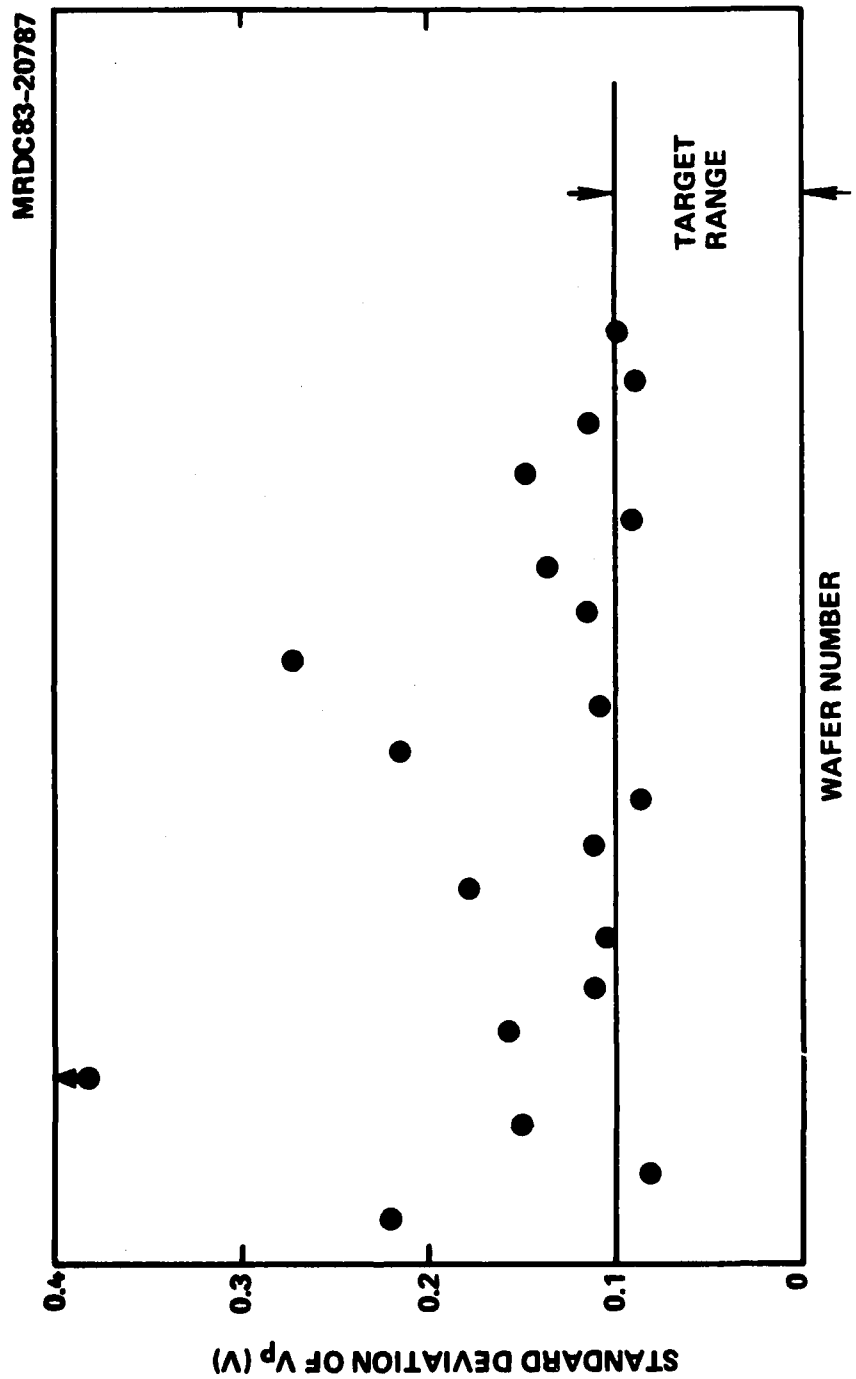


Fig. 5.2-2 Standard deviation over 3 in. wafers of FET pinchoff voltage V_p for initial 3 in. RAM wafers.

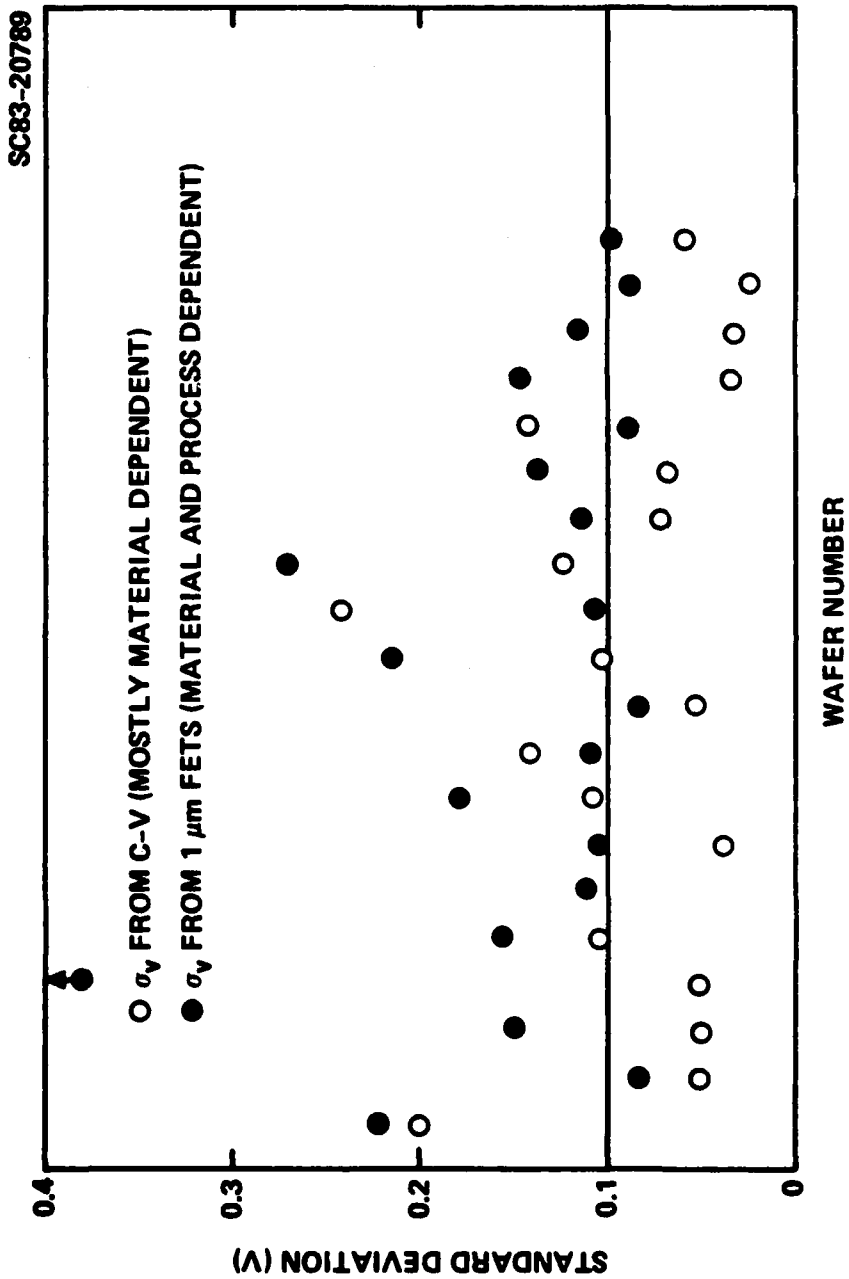


Fig. 5.2-3 Comparison of uniformity of depletion voltage and pinchoff voltage for initial 3 in. RAM wafers.

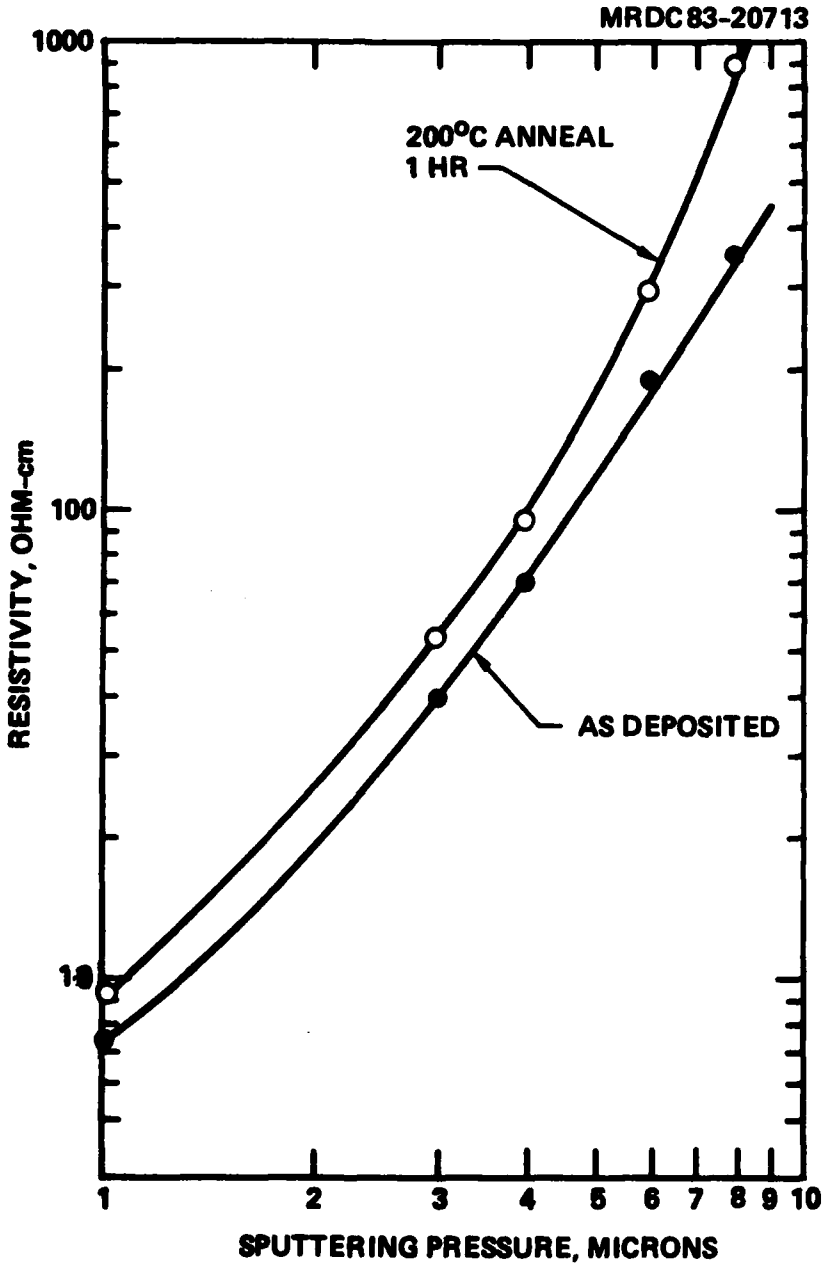


Fig. 5.2-4 Cermt resistivity as a function of sputtering pressure.

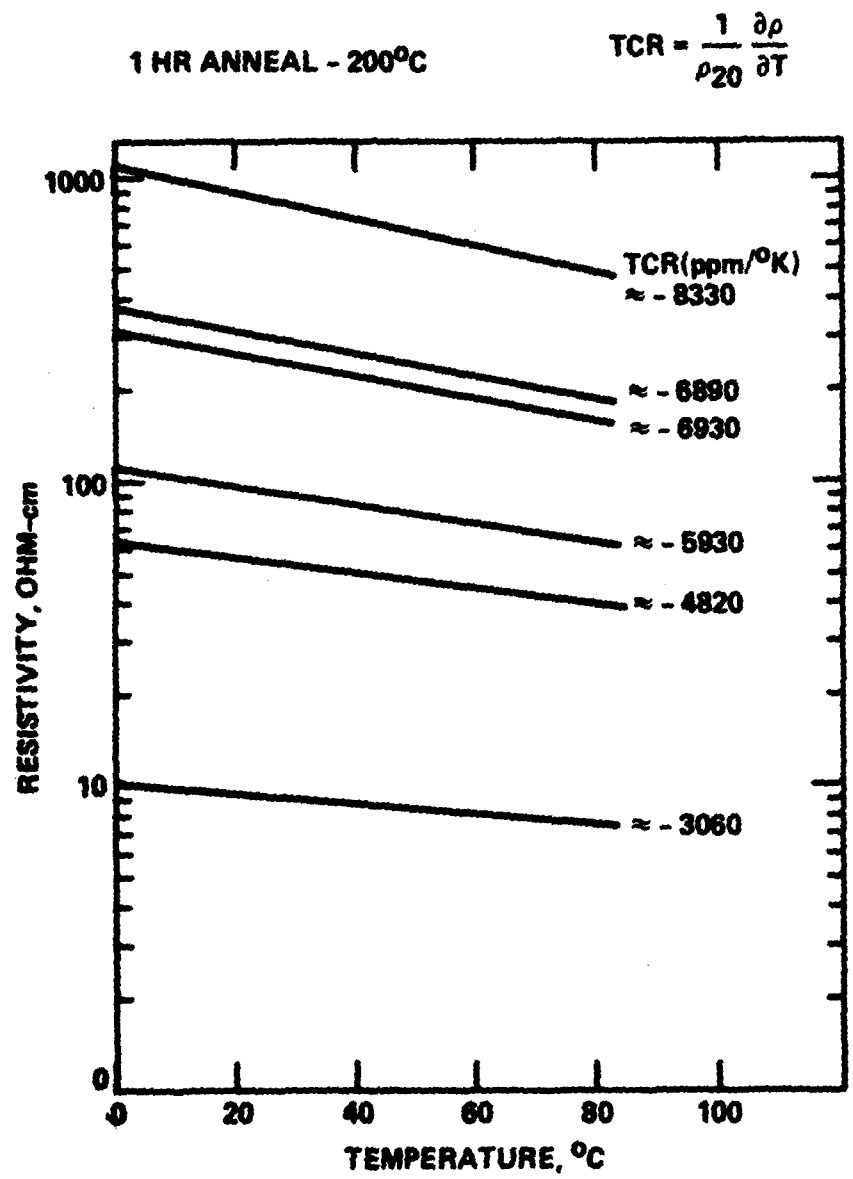


Fig. 5.2-5 Resistivity vs temperature for temperature coefficient evaluation.

other reported results,[2] and should not pose a threat to the operation of the RAM cell.

In general, the RAM process for 3 inch wafers proved to be acceptable for producing fully functional 256 bit arrays. A photograph of a completed 256 bit array is shown in Fig. 5.2-6. For the first six wafer lots completed, a process yield of 63% was obtained. Wafer breakage was the main yield limiting factor, and is expected to decrease as more experience in handling 3 in. wafers is gained.

5.3 Test Results from Mask Set RM3

The results from testing wafers fabricated with mask set RM3 are important in two ways. First, this was the first demonstration of the successful fabrication of 3-inch GaAs wafers. Second, this was the first demonstration of a fully functional 256-bit RAMs. The testing of circuits on wafers from mask set RM3 comprised yield analysis discussed in Sec. 5.3.1, analysis of the operation of the peripheral circuits discussed in Sec. 5.3.2, and finally the testing of fully decoded 256-bit RAMs discussed in Sec. 5.3.3.

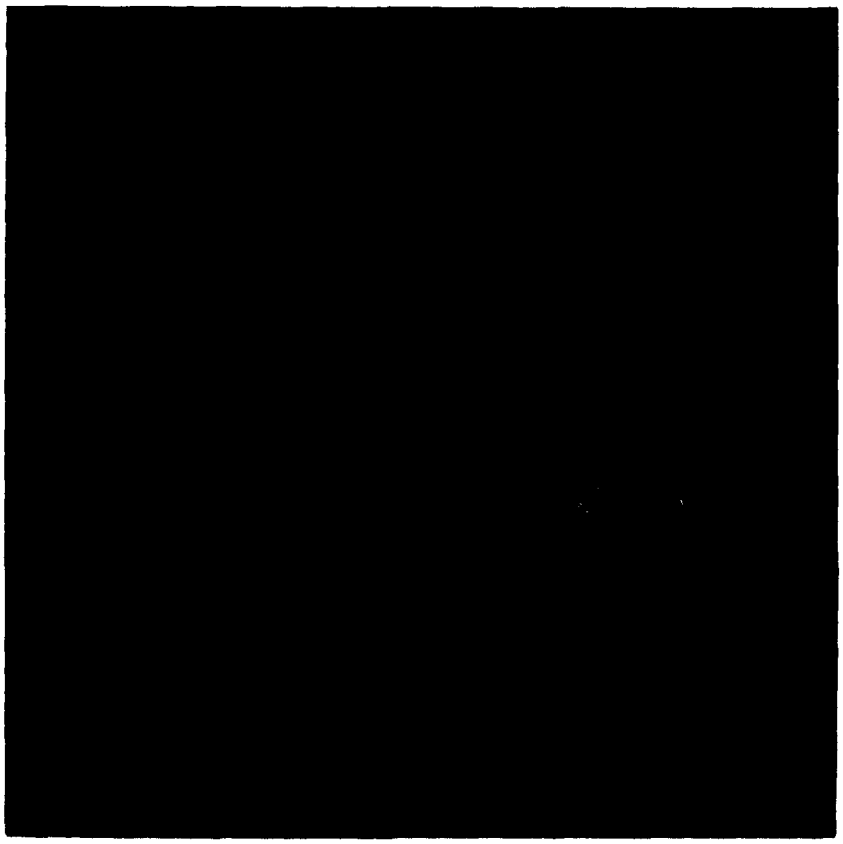
5.3.1 RAM Cell Analysis

Since the RAM cell used on mask set RM3 is almost identical to the one used on mask set RM2, the operation of this cell had already been characterized. It had been determined that this cell was sensitive to leakage due to the very low currents involved, and that proton bombardment of the unimplanted substrate areas provided a good cure for leakage. The analysis carried out at this stage dwelled on more subtle possible failure mechanisms.

Four possible failure mechanisms were considered. These were residual substrate leakage, unbalance of the load resistors, unbalance of the speed-up capacitors, and nonuniformity of the threshold voltage. These four possible causes for cell failure are discussed in the rest of the section.

MRDC83-21378

256 BIT GaAs STATIC RAM



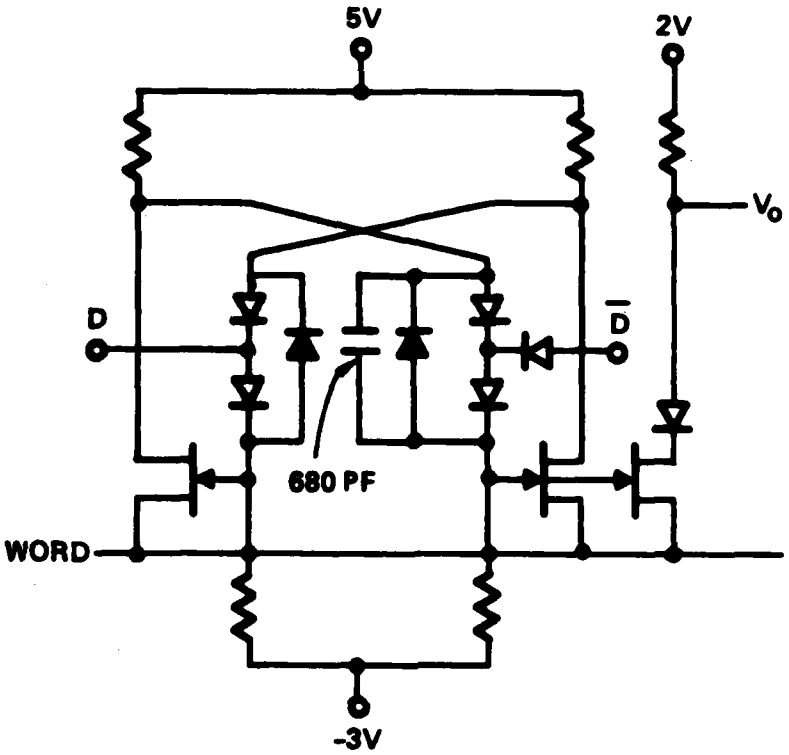
1.3 x 1.3 mm

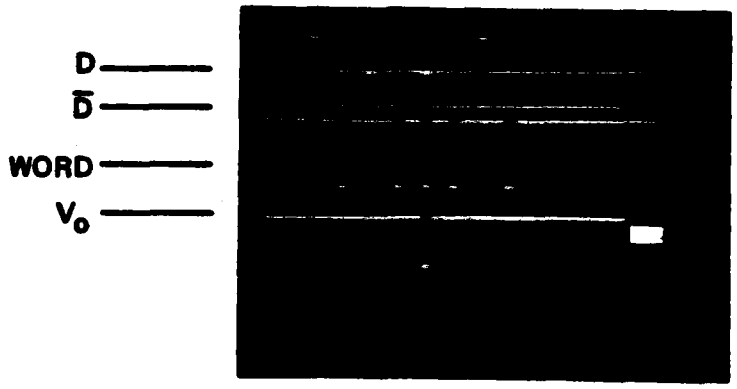
Fig. 5.2-6 256 bit GaAs static RAM.

1. Residual Substrate Leakage. This topic was already discussed in context of mask set RM2 when its importance was discovered. For the moment proton bombardment seems to provide a good correction of the leakage problems. Although the correction is in general effective, the possibility still remains that individual cells may still suffer from some residual leakage. For the moment there is no indication that this should happen, but this possibility will be considered in any future yield investigation.

2. Resistor Unbalance. All mask sets in this program have been provided with test structures to measure the sheet resistance of the cermet resistor layer, and the total resistance of resistors identical to those used in the circuit. The results from characterizing the test structure have been very satisfactory. Standard deviations of total resistance on the order of 10% of the average value are quite common. With this very low standard deviation across a whole wafer, the possibility of any large unbalance of load resistors within a cell is very unlikely.

3. Unbalance of Speed-Up Capacitors. As shown in Fig. 5.1-2, the fast operation of the RAM cell requires speed-up capacitors in the cross connections between the two FETs. The level shifting diodes in those cross connections provide some capacitance, but most of the capacitance needed, as shown in Fig. 5.1-2, is obtained by adding two reverse biased diodes labeled D1 and D2. An additional dielectric capacitor not shown on the figure is also used. To test whether unbalance of these capacitors could prevent the cell from storing information, test circuits containing single memory cells with all their nodes connected to contacts were used. As shown on Fig. 5.3-1, an external capacitor was added to one of the cross connections and its value was varied. Write and read operations were performed to determine whether the cell was able to latch the correct value. The threshold for causing a failure was found to be very high. A 680 pF capacitor had to be used to cause a failure, since such a value is several orders of magnitude larger than the capacitance of the diodes and capacitors used in the cell. Unbalance of capacitors was ruled out as a likely cause of failures.



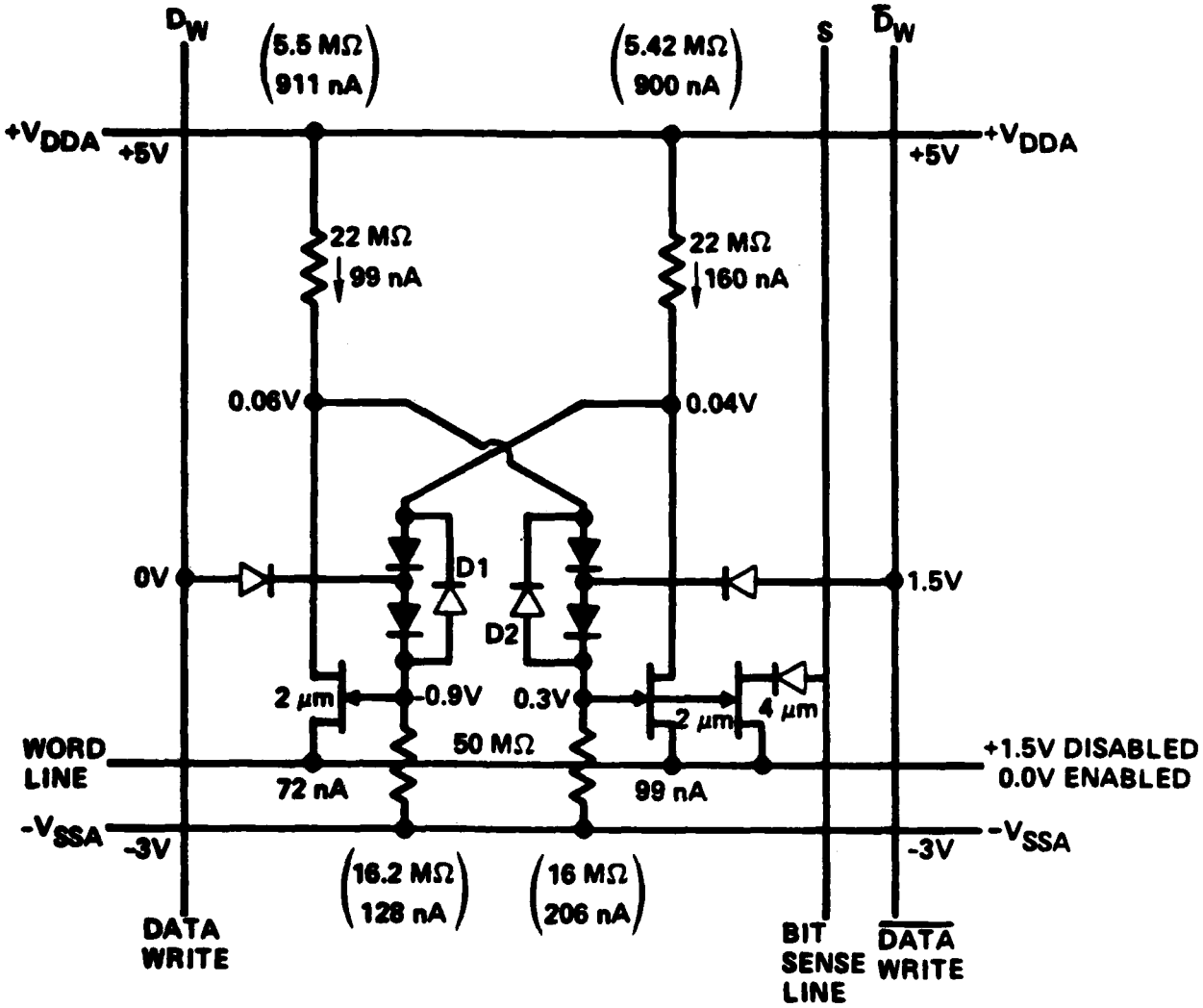


680 pF CAPACITOR ACROSS V_D^L & V_g^R NEEDED TO FAIL TO STORE "0"

Fig. 5.3-1 Artifical unbalance of the speed-up capacitors ina 256 bit RAM cell.

4. FET Threshold Voltage Uniformity. Variations of MESFET threshold voltage can cause failures because they may prevent certain transistors from turning on or off. Test memory cells on which each electrical node could be probed were evaluated looking for failures due to threshold voltage variations. Figure 5.3-2 shows an example of such failure. On this figure, the nominal resistor and current values are shown on a schematic of the cell. Measured voltages at drains and sources of the transistors are also shown for the condition where a zero is being stored. Under this condition, the left transistor should be off and the right transistor should be on. The gates of the transistor are indeed in the required state because the D_w and the $\overline{D}_w$ lines are being held at 0 and 1.5 V, respectively, by the external write circuit. However, despite the -0.9 V applied to the gate of the left transistor, this is still, as shown by its low drain voltage, 0.06 V, very close to the 0 V source voltage. The right transistor is on as expected. It is obvious that as soon as the D_w and $\overline{D}_w$ voltages are removed, the gate voltage on the right transistor will not remain at 0.3 V, but will drop and the latch will reach some undetermined state with both transistors on. The fact that the left transistor is on despite having -0.9 V applied to its gate is due to its threshold voltage. Although it cannot be measured directly on the cell, neighboring parametric test cells show that the FET threshold voltage in this area of the wafer is ~ -0.9 V. Due to subthreshold currents, the transistor is still conducting enough current to be considered on when its gate is biased at its nominal threshold voltage. A gate bias ~ 0.2 V lower than the nominal transistor threshold voltage is required to turn a transistor off at the low current levels employed.

The results of a caculation of permissible threshold voltages is shown in Fig. 5.3-3. Here, the highest absolute value for the allowed threshold voltage is displayed as a function of the pull-down resistor value and the negative supply voltage. The figure shows that the larger the value of the pull-down resistor or the lower the negative supply voltage, the smaller the margin allowed for the negative threshold voltage of the FET. For the RM3



FAILURE TO STORE "0"

EXCESS "I_D^L", V_T OF LFET, $V_T \cong -0.9$

Fig. 5.3-2 Example of cell failure due to an excessively high threshold voltage.

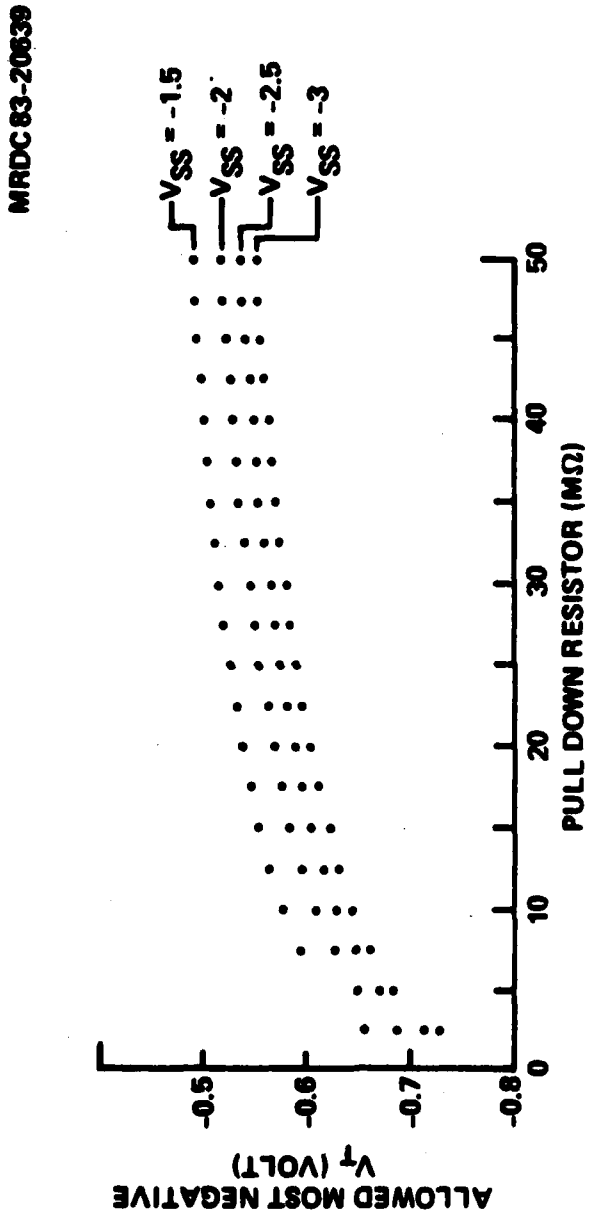


Fig. 5.3-3 Calculated dependance of the most negative FET threshold voltage on pull-down resistor value and negative supply voltage.

design values of $R_{pull-down}$ = 50 MΩ and V_{SS} = -3 V, the allowed negative threshold voltage is -0.55 V. The value in the example of the previous paragraph was obviously well beyond the acceptable margin. Figure 5.3-3 indicate that it is possible to lower the pull-down resistor value and the supply voltages at the same time without changing the sensitivity to threshold voltages. Therefore, it is possible to maintain the same power consumption of the cell with higher current values resulting in lower sensitivity to leakage without affecting the sensitivity to FET threshold voltage.

The overall conclusion from the analysis discussed above is that threshold voltage uniformity apear to the most sensitive parameter which may control the yield of RAM cells.

5.3.2 Peripheral Circuit Analysis

Mask set RM3 provided an opportunity to test each component of the peripheral circuits since they had been placed in test areas with all the most significant electrical nodes connected to probe pads. The conclusion reached after extensive testing was that these circuits are more sensitive to backgating than what had been expected. This is probably due to the low threshold voltages used, which tend to make any FET threshold shift due to backgating relatively more significant than with larger threshold voltages. Proton bombardment was found to improve the operating conditions of the circuits by reducing the backgating effect. However, even with proton bombardment the operation of the peripheral circuits was still rather marginal. Although sufficient to accomplish full operation of the RAM, the need for a new design iteration became quite obvious.

The row decoder provides a good example of the experimental analysis carried out on the peripheral circuits. A schematic of this circuit is shown on the upper portion of Fig. 5.3-4. The lower part of the figure displays the voltage at node A, which is the gate of the switching FETs in the complementary driver, as a function of the negative supply voltage. It is important to remember that the value of V_{SS} [illegible] negative supply voltage controls the mag

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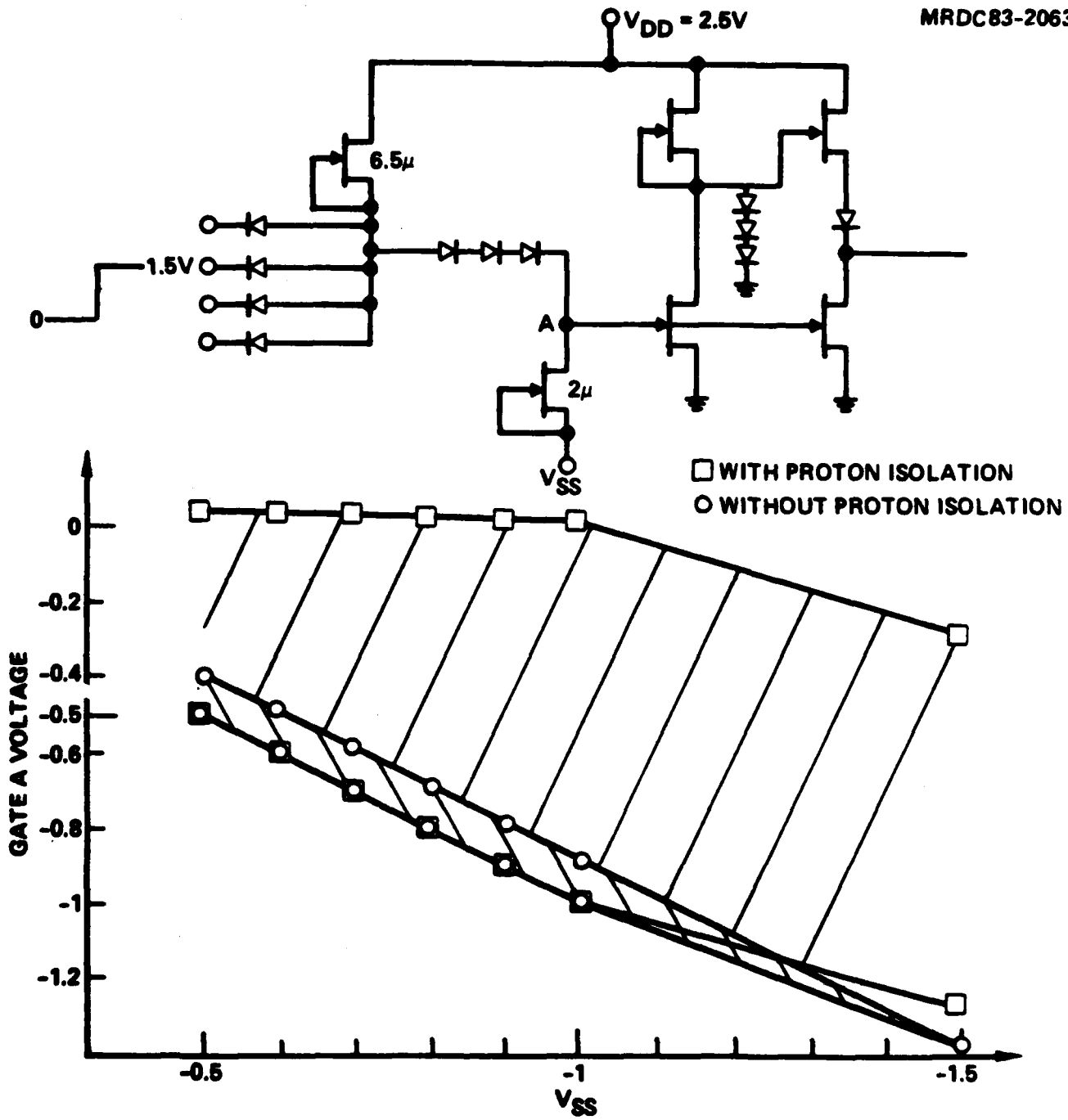


Fig. 5.3-4 Effects of backgating voltage on the operating characteristics of a row decoder circuit with and without proton bombardment.

nitude of the backgating effect. If backgating did not exist, the curves on Fig. 5.3-4 would be just two well-separated straight horizontal lines because the supply voltage, V_{SS}, is in series with a current limiter. Instead, if proton isolation is not used, the two curves are not only slanted, but they are also very close to each other and almost no switching takes place. Proton bombardment makes a significant difference. By reducing the magnitude of the backgating effect with proton bombardment, it causes a clear distinction to appear between the on and off state, as shown in Fig. 5.3-4. Under this condition, the circuit can be made operational if properly biased.

Although proton bombardment alleviates backgating, it is possible to design for backgating so that the circuit is less dependent on proton bombardment. This was demonstrated on the row decoder circuit just discussed. Backgating on Fig. 5.3-4 manifested itself by the 6.5 μm wide pull-up resistor at the input of the decoder not being capable to supply enough current due to the reduction of its current carrying capability. The performance of the circuit can be improved by simply making this pull-up wider so that it can carry more current. This was demonstrated by a small mask modification on a test structure. This modification, which was possible because the masks are ten times larger than the final pattern, consisted of removing the gate from the 6.5 μm pull-up FET and converting it into a saturated resistor as shown on the upper portion of Fig. 5.3-5. With every other dimension and process parameter left unchanged, the saturated resistor is equivalent to a 3 times wider FET pull-up. As a result of this change, a dramatic change takes place in the operating characteristics of the row decoder as shown on the lower portion of Fig. 5.3-5. A larger positive high value is obtained for the voltage node A, and most importantly, a well defined low state is also obtained. With this design change, the proton bombardment had only a small insignificant effect.

Unfortunately, the correction discussed above could only be made on a test structure. It was impractical to make a manual mask corection on all 16 row decoders of the actual RAMs. However, this experiment provides useful information for the design iteration made on the following mask set. Similar

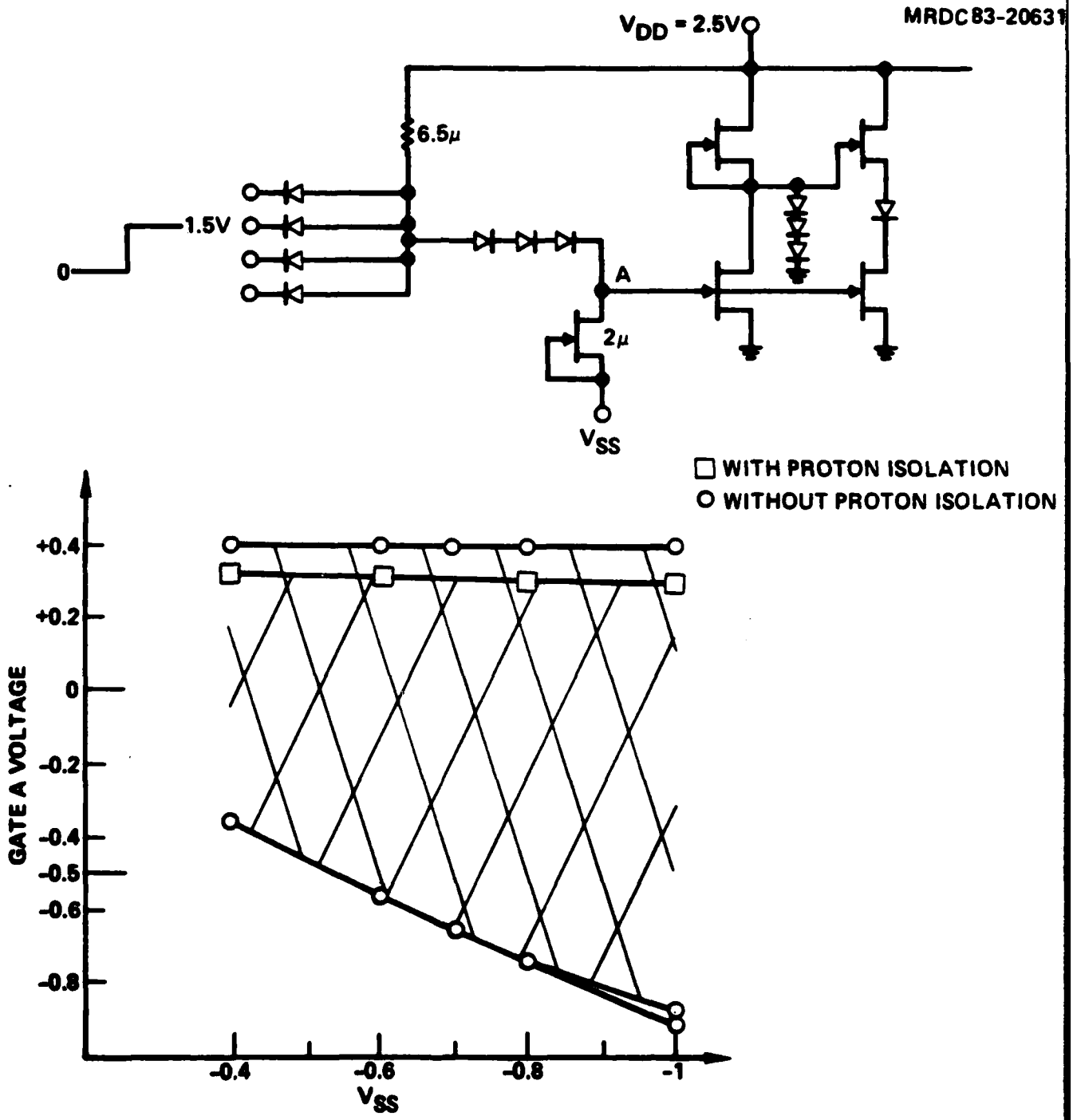


Fig. 5.3-5 Improved backgating sensitivity of the row decoder after a design correction (the pull-up active load was replaced by a saturated resistor).

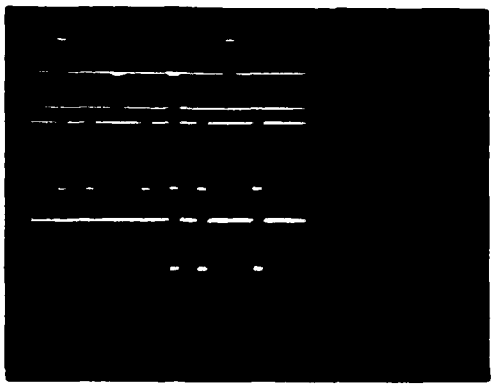
backgating limitations were observed on the column decoders and the sense amplifier. However, with the help of proton bombardment and a good understanding of the operational limits of each component, it was possible to determine the optimum bias conditions required to successfully operate the 256-bit RAM.

5.3.3 Testing of Fully Decoded 256-Bit RAMs

The functionality of the 256-bit static RAMs was tested using a lab microcomputer equipped with analog and digital outputs and inputs. The functionality tests were conducted at low speeds, limited by the lab microcomputer which was controlling the measurement. The test pattern used is illustrated in Fig. 5.3-6. The test procedure consists of write enabling one cell, writing a "one" in it, and disabling it. A "zero" is then written in a neighboring cell. After this is done, the original cell is enabled and read back to verify whether it held the "one" without being disturbed by the write operation in the neighboring cell. The process is then repeated writing a "zero" in the cell and a "one" in its neighbor. A cell was considered functional only if it passed both tests. In practice, this test pattern resembles very much a "walking one," and a "walking zero" pattern.

The yield of functional 256-bit static RAMs was measured on wafer. The results are summarized in Table 5.3-1 along with the average and standard deviation of threshold voltage for each wafer. The number of totally functional 256-bit RAMs is low. However, this yield is affected by the rather marginal operation of the peripheral circuits. Note the large number of failures in the range of 15 to 100. This number is larger than the number of failures for over 100 cells for most of the wafers. This anomaly is due to the large number of failures caused by the peripheral circuits, which occur by multiples of 16 cells, since the memory is arranged by a 16 × 16 array.

The column labeled testable chips in Table 5.3-1 indicates the percentage of chips which had no obvious failure, and on which it was worth conducting a functionality test. This column indicates a very large number of



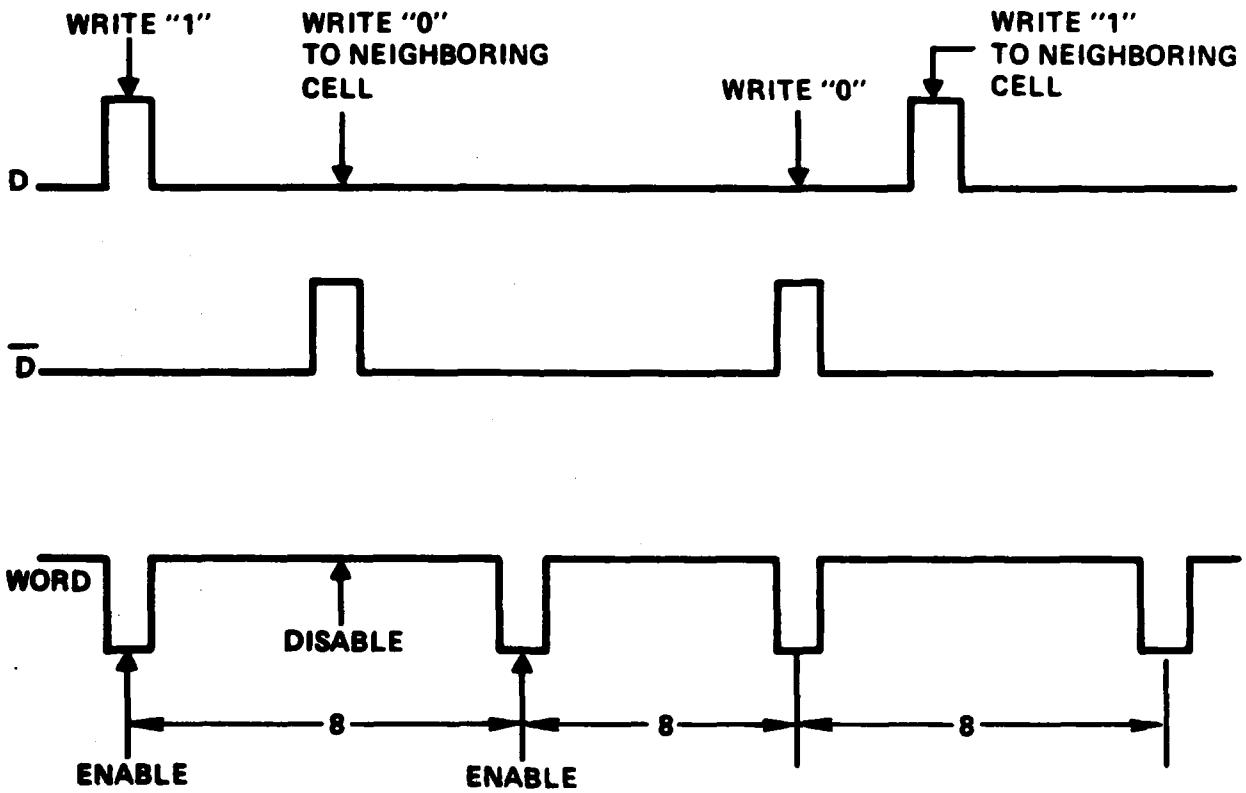


Fig. 5.3-6 Pattern for functionality testing of 256 bit static RAMs.

rejections. Mask set RM3, on which these RAMs were fabricated, was the first mask set used with a wafer stepper to process 3-inch GaAs wafers. The large number of losses was due to failures in the alignment, most of the time gross failures caused by lack of experience with the design of alignment marks. This problem has been corrected in subsequent mask sets.

Table 5.3-1
Yield of Decoded 256-Bit RAM Chips

Wafer Number	Number of Cell Failures						Testable Chips	Remarks
	0	1	2	3-14	15-100	> 100		
51				2	5	10	8%	$V_T \cong 0.71 \pm 1.12$ V
52	4	5	2	6	41	38	44%	$V_T \cong 0.65 \pm 0.11$ V
54						11	5%	Lithography limited
62	8	7	3	8	47	27	45%	$V_T \cong 0.67 \pm 0.12$ V
63	1			7	24	6	17%	Lithography limited

The power consumption of this static RAM is typically between 200 and 250 mW. Almost all this power consumption takes place in the peripheral circuits which were not designed for low power dissipation. A drastic reduction will be attempted with the next design iteration. This will be accomplished by replacing source follower drivers by complementary drivers, optimizing the design, and incorporating a power down switch which will turn off the peripheral circuits when the chip is not addressed.

The access time was measured on individual cells at random, due to lack of instrumentation capable of automatically testing GaAs high speed RAMs at full speed. The methodology and the result of a read access time measurement is illustrated in Fig. 5.3-7. As shown on the top portion of this fig

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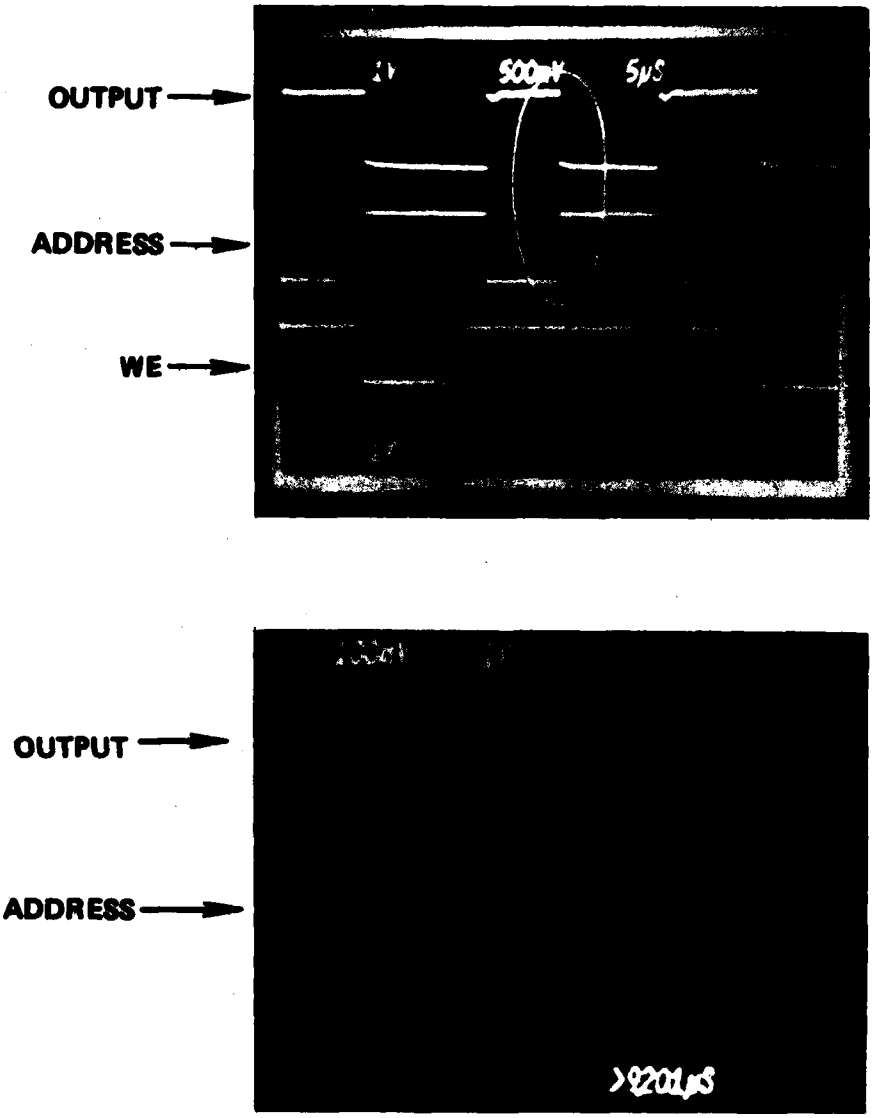


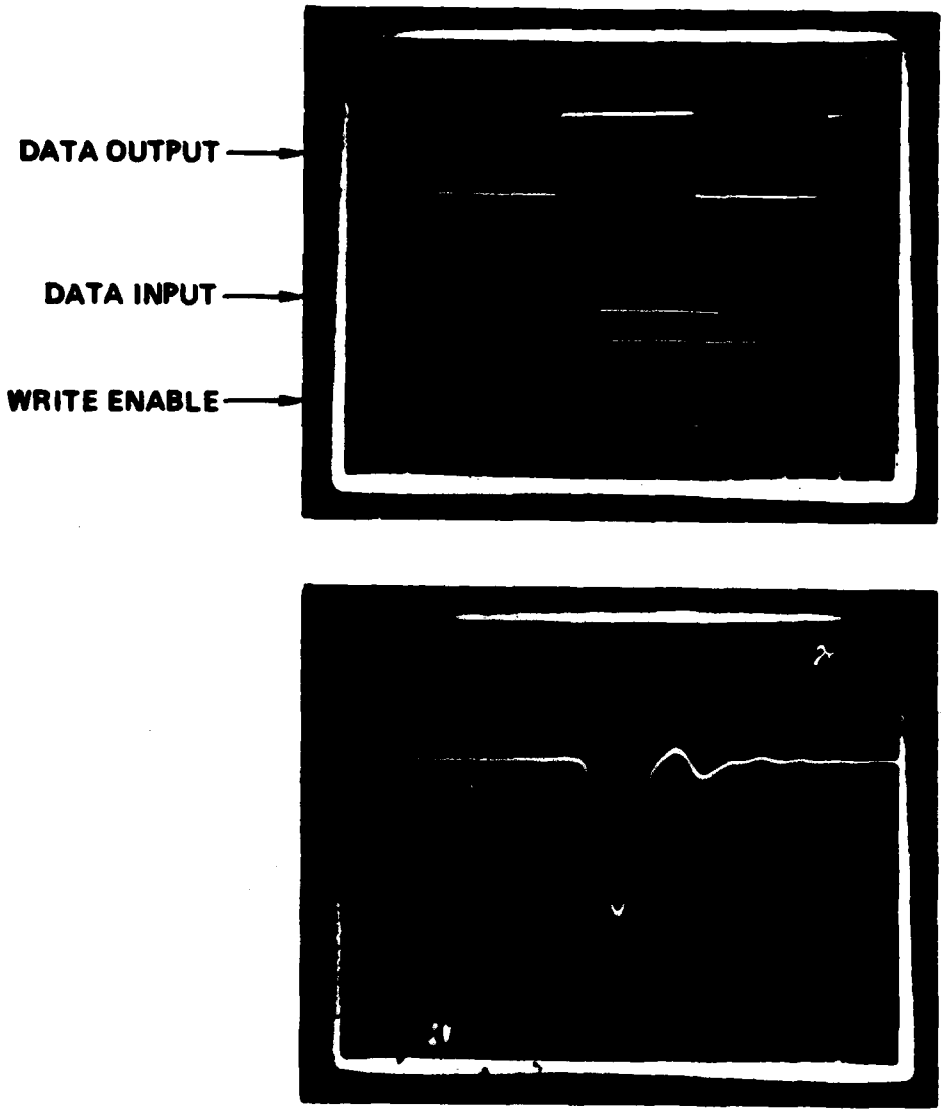
$\tau \simeq 1.0$ ns

Fig. 5.3-7 Read access time measurement on a 256 bit static RAM.

ure, the output is monitored continuously, and to do so the "read enable" line is constantly enabled. All the address lines are kept unchanged except for one bit which is toggled back and forth. At the start of a cycle, when the address is changed, the "write enable" line is turned on, and a "zero" is written in the cell, as confirmed by the output signal. The "write enable" line is then turned off, and the address is changed. When the address changes, the output also changes because a different cell is being read. Finally, the address is changed back to the original one, and the output follows the change of address displaying the zero that was stored in the cell. The access time is measured between the midpoint of the transition of the address and the midpoint of the transistion of the output. These two waveforms are displayed on an expanded scale on the lower part of Fig. 5.3-7. This example corresponds to a typical measurement which yields a read access time of 8 ns.

As to the write operation, an important parameter is the minimum width of the write pulse required for the cell to store a bit. A "write" pulse width measurement is illustrated in Fig. 5.3-8. As with the access time measurement, the output is monitored continuously with the "read enable" line permanently on. The address is kept unchanged while the data input is switched periodically between "one" and "zero". The write enable line is turned on for a very short time in the second half of the data input cycle. As shown by the top trace on Fig. 5.3-8 the output changes whenever this "write enable" pulse is turned on showing that the pulse length is sufficient for the input data to be acquired by the cell. The experiment consists of shortening this write enable pulse, and determining at what length it becomes too short for the cell to latch in the new data. In this measurement, the pulse was shortened to the minimum length allowed by the test equipment, 2 ns, without observing failures.

The result from the high speed measurements on the 256-bit RAM indicate that this chip is indeed capable of operating at high speed. This should not be surprising because the peripheral circuits used in this 256-bit version consume rather high power, and therefore they should be expected to operate at



WRITE PULSE WIDTH < 2 ns

Fig. 5.3-8 Measurement of the minimum "write enable" pulse width on a 256 bit static RAM.

high speed. More significant is the ability of the low power RAM cell to, indeed, operate at high speed. In particular, the ability of the cell to store a "one" or a "zero" with a very short (2ns) "write" pulse is very important, because it leaves 8 ns to the peripheral circuit for all the rest of the write operation.

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